Rockwell

R65C52 DUAL ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (DACIA)

PRELIMINARY

DESCRIPTION

The Rockwell CMOS R65C52 Dual Asynchronous Communications Interface Adapter (DACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The DACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 38,400 baud, or at 1/16 times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at 1/16 times the external clock rate. The DACIA is programmable for word lengths of 5, 6, 7 or 8 bits; even, odd, or no parity; and 1 or 2 stop bits.

The DACIA is designed for maximum programmed control from the microprocessor (MPU) to simplify hardware implementation. Dual sets of registers allow independent control and monitoring of each channel. The DACIA also provides a unique, programmable Automatic Address Recognition Mode for use in a multidrop environment.

The Control Register and Status Register permit the MPU to easily select the R65C52's operating modes and determine operational status.

The Interrupt Enable Registers (IER) and Interrupt Status Registers (ISR) allow the MPU to control and monitor the interrupt capabilities of the DACIA.

The Control and Format Register (CFR) permits selection of baud rates, word lengths, parity and stop bits as well as control of DTR and RTS output signals.

The Status Register (SR) gives the MPU access to the state of the modem control lines, framing error, transmitter underrun and break conditions.

The Compare Data Registers (CDR) hold the data value to be used in the compare mode and the Transmit Break Register (TBR) commands a Transmit Break and provides for parity/address recognition, for Automatic Address Mode.

The Transmitter Data Register and Receiver Data Register are used for temporary data storage of input and output data.

FEATURES

- Low power CMOS N-well silicon gate technology
- Two independent full duplex channels with buffered receivers and transmitters.
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 38,400)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Programmable control of edge detect for DCD, DSR, DTR, RTS, and CTS
- Program-selectable serial echo mode for each channel
- Automatic Address Recognition Mode for multi-drop operation.
- Up to 4 MHz host bus operation
- 5.0 Vdc ±5% supply requirements
- 40-pin plastic or ceramic DIP
- Full TTL or CMOS input/output compatibility
- Compatible with R6500 and R65C00 microprocessors and R6500/* microcomputers.

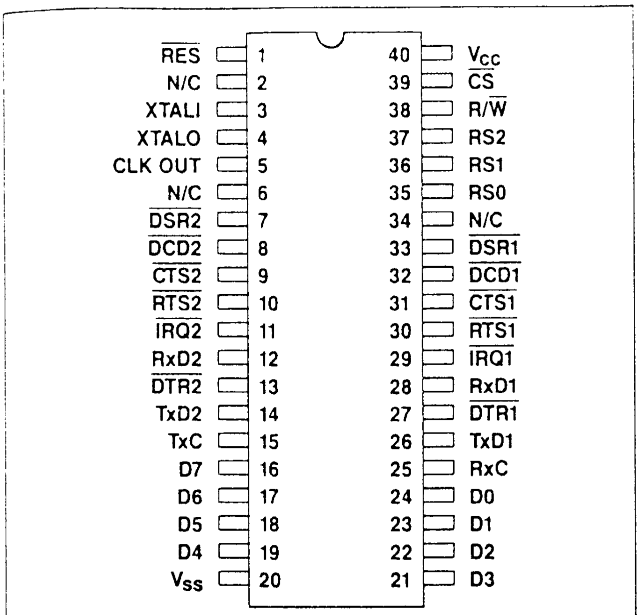
ORDERING INFORMATION

Part Number:
R65C52 _ _ _

Temperature Range (T_L to T_H):
Blank = 0°C to +70°C
E = −40°C to +85°C

Frequency Range:
2 = 2 MHz
4 = 4 MHz

Package
C = Ceramic
P = Plastic



Note: N/C indicates no connection

Figure 1. R65C52 Pin Configuration

INTERFACE SIGNALS

Figure 2 shows the DACIA interface signals associated with the microprocessor and the modem.

DATA BUS (D0–D7)

The D0–D7 pins are eight data lines that transfer data between the microprocessor (MPU) and the DACIA. These lines are bidirectional and are normally high-impedance except during READ cycle when the DACIA is selected.

REGISTER SELECTS (RS0, RS1, RS2)

The three register select lines are normally connected to the processor address lines to allow the MPU to select the various internal registers. Table 1 shows the internal register select coding and identifies the abbreviations (ABBR) used throughout the text for each register.

READ/WRITE ($R/\overline{W}$)

The $R/\overline{W}$ input, generated by the microprocessor, controls the direction of data transfer. A high on the $R/\overline{W}$ line indicates a read cycle, while a low indicates a write cycle.

CHIP SELECT ($\overline{CS}$)

The chip select input is normally connected to the processor address lines either directly or through decoders. The DACIA latches address and $R/\overline{W}$ inputs on the falling edge of $\overline{CS}$ and latches the data bus inputs on the rising edge of $\overline{CS}$.

RESET ($\overline{RES}$)

During system initialization a low level on the $\overline{RES}$ input causes a RESET to occur. At this time the IER's are set to \$80, the $\overline{DTR}$ and $\overline{RTS}$ lines go to the high state, the RDR register is cleared, the TBR is set to \$0F, the compare mode is disabled, and the $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ flags are cleared. No other bits are affected.

TRANSMIT DATA (TXD1, TXD2)

The TxD outputs transfer serial non-return to zero (NRZ) data to the data communications equipment (DCE). The data is transferred, LSB first, at a rate determined by the baud rate generator.

RECEIVE DATA (RXD1, RXD2)

The RxD inputs transfer serial NRZ data into the DACIA from the DCE, LSB first. The receiver baud rate is determined by the baud rate generator.

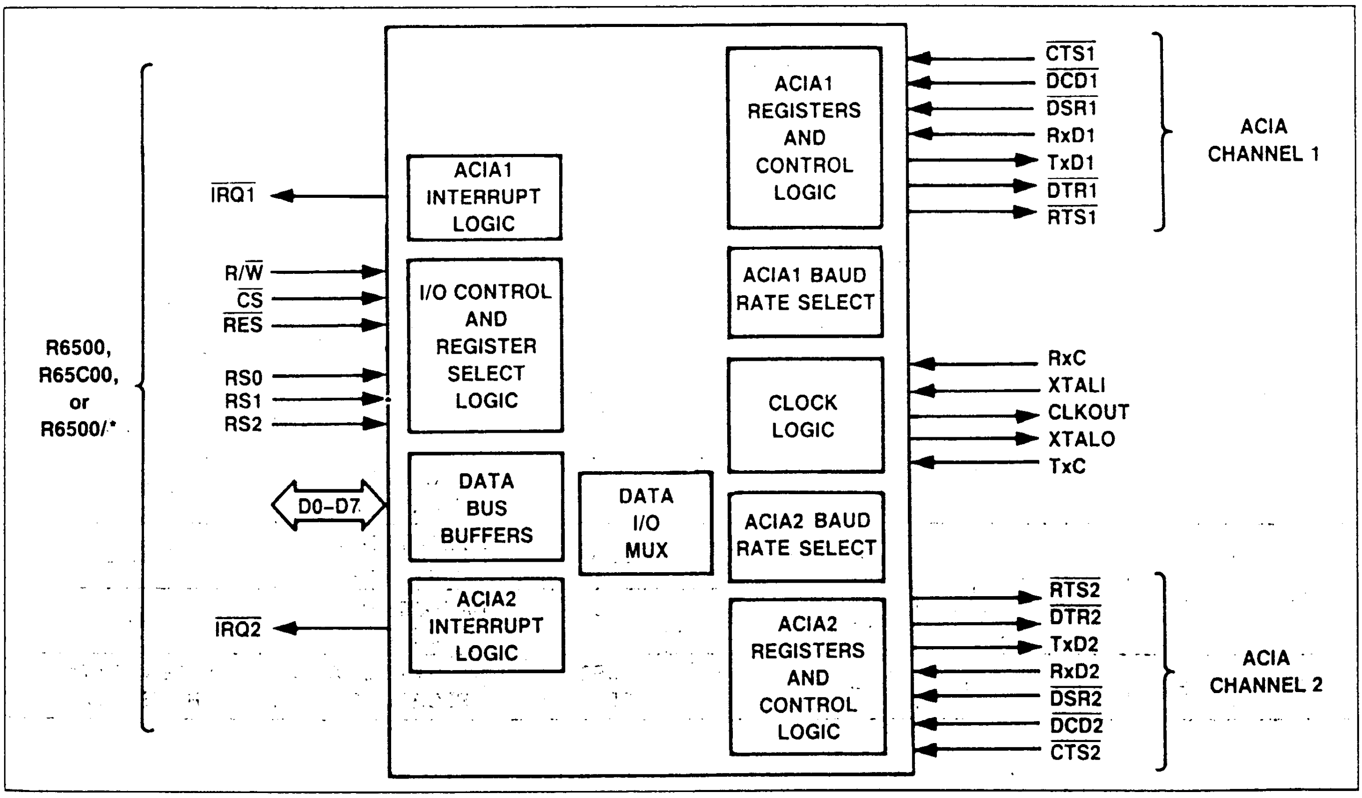


Figure 2. DACIA Interface Signals

CLEAR TO SEND ($\overline{\text{CTS1}}$, $\overline{\text{CTS2}}$)

The $\overline{\text{CTS}}$ control line inputs allow handshaking by the transmitter. When $\overline{\text{CTS}}$ is low, the data is transmitted continuously. When $\overline{\text{CTS}}$ is high, the Transmit Data Register empty bit in the ISR is not set. The word presently in the Transmit Shift Register is sent normally. Any active transition on the $\overline{\text{CTS}}$ lines sets the $\overline{\text{CTS}}$ bit in the appropriate ISR. The $\overline{\text{CTS}}$ status bit in the CSR reflects the current high or low state of $\overline{\text{CTS}}$.

DATA CARRIER DETECT ($\overline{\text{DCD1}}$, $\overline{\text{DCD2}}$)

These two lines may be used as general purpose inputs. An active transition sets the $\overline{\text{DCD}}$ bit in the ISR. The $\overline{\text{DCD}}$ bit in the CSR reflects the current state of the $\overline{\text{DCD}}$ line.

DATA SET READY ($\overline{\text{DSR1}}$, $\overline{\text{DSR2}}$)

These two lines may be used as general purpose inputs. An active transition sets the $\overline{\text{DSR}}$ bit in the ISR. The $\overline{\text{DSR}}$ bit in the CSR reflects the current state of the $\overline{\text{DSR}}$ line.

REQUEST TO SEND ($\overline{\text{RTS1}}$, $\overline{\text{RTS2}}$)

These two lines may be used as general purpose outputs. They are set high upon reset. Their state may be programmed by setting the appropriate bits in the CFR high or low. The state of the $\overline{\text{RTS}}$ line is reflected by the $\overline{\text{RTS}}$ bit in the CSR.

DATA TERMINAL READY ($\overline{\text{DTR1}}$, $\overline{\text{DTR2}}$)

These two lines may be used as general purpose outputs. They are set high upon reset. Their state may be programmed by setting the appropriate bits in the CFR high or low. The state of the $\overline{\text{DTR}}$ line is reflected by the $\overline{\text{DTR}}$ bit in the CSR.

INTERRUPT REQUEST ($\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$)

The $\overline{\text{IRQ}}$ lines are open-drain outputs from the interrupt control logic. $\overline{\text{IRQ1}}$ is associated with ACIA1 and $\overline{\text{IRQ2}}$ is associated with ACIA2. These lines are normally high but go low when one of the flags in the ISR is set, provided that its corresponding enable bit is set in the IER.

Table 1. DACIA Register Selection

HEX ADDR	REGISTER SELECT LINES RS2	RS1	RS0	CONTROL AND FORMAT REGISTER BITS CFR-7	CFR-6	REG ABBR	REGISTER ACCESS WRITE	READ
00	L	L	L	—	—	IER1 ISR1	INTERRUPT ENABLE REGISTER 1	INTERRUPT STATUS REGISTER 1
01	L	L	H	0	—	CFR1 SR1	CONTROL REGISTER 1	STATUS REGISTER 1
				1	—	CFR1	FORMAT REGISTER 1	INVALID
02	L	H	L	—	0	CDR1	COMPARE DATA REGISTER 1	INVALID
				—	1	TBR1	TRANSMIT BREAK REGISTER 1	INVALID
03	L	H	H	—	—	TDR1 RDR1	TRANSMIT DATA REGISTER 1	RECEIVE DATA REGISTER 1
04	H	L	L	—	—	IER2 ISR2	INTERRUPT ENABLE REGISTER 2	INTERRUPT STATUS REGISTER 2
05	H	L	H	0	—	CFR2 SR2	CONTROL REGISTER 2	STATUS REGISTER 2
				1	—	CFR2	FORMAT REGISTER 2	INVALID
06	H	H	L	—	0	CDR2	COMPARE DATA REGISTER 2	INVALID
				—	1	TBR2	TRANSMIT BREAK REGISTER 2	INVALID
07	H	H	H	—	—	TDR2 RDR2	TRANSMIT DATA REGISTER 2	RECEIVE DATA REGISTER 2

FUNCTIONAL DESCRIPTION

Figure 3 is a block diagram of the DACIA which consists of two asynchronous communications interface adapters with common microprocessor interface control logic and data bus buffers. The individual functional elements of the DACIA are described in the following paragraphs.

INTERRUPT LOGIC

The interrupt logic causes the $\overline{IRQ}$ lines ($\overline{IRQ1}$ or $\overline{IRQ2}$) to go low when conditions are met that require the attention of the MPU. There are two registers (the Interrupt Enable Register and the Interrupt Status Register) involved in the control of interrupts in the DACIA. Corresponding bits in both registers must be set to cause an $\overline{IRQ}$.

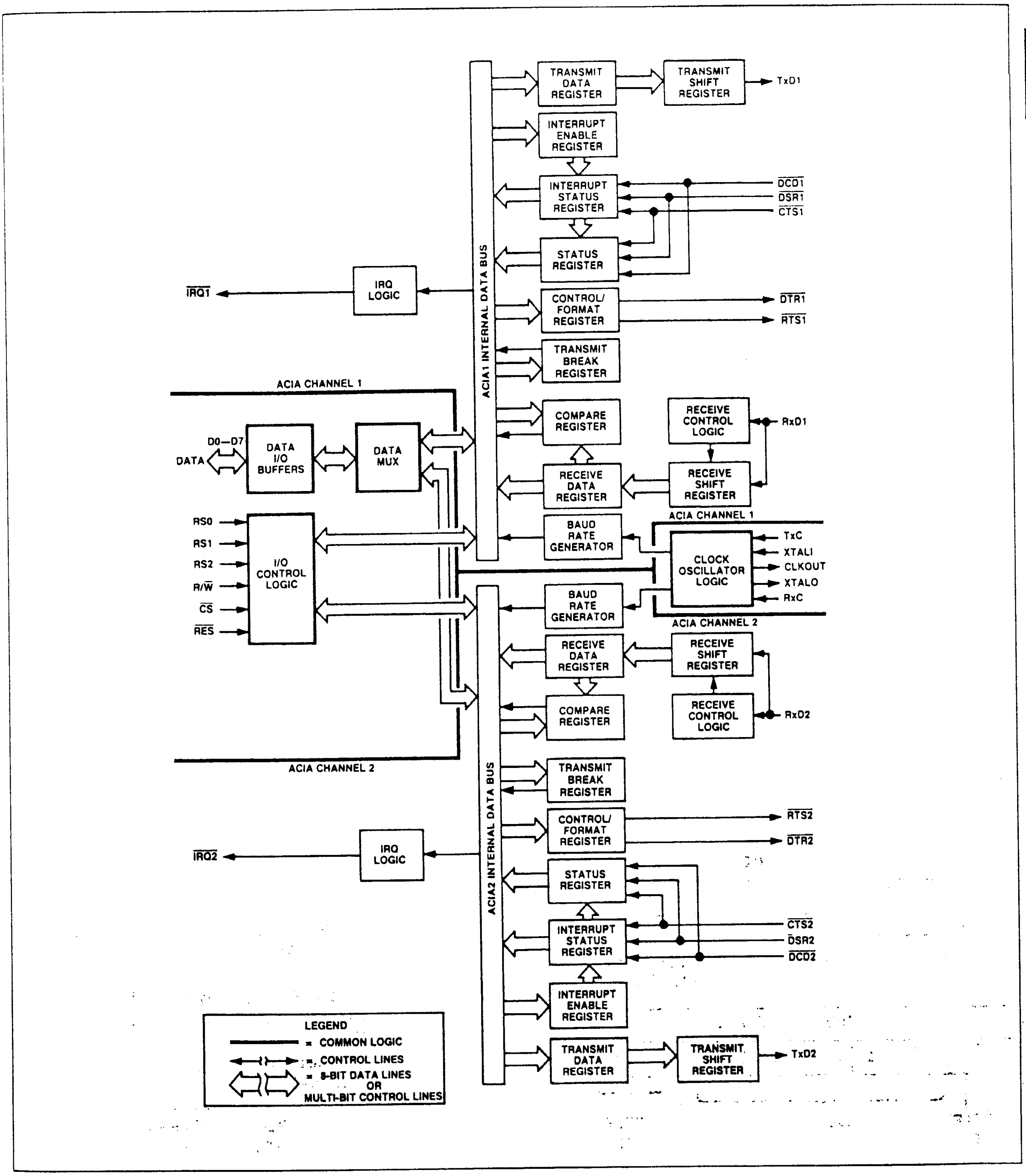


Figure 3. DACIA Block Diagram

DATA BUS BUFFER

The Data Bus Buffer is a bidirectional interface between the system data lines and the internal data bus. When R/$\overline{W}$ is low and $\overline{CS}$ is low, the Data Bus Buffer writes data from the internal data bus to the system data lines. When R/$\overline{W}$ is high and $\overline{CS}$ is low, data is driven into the DACIA from the system data bus. Table 2 summarizes the Data Bus Buffer states.

Table 2. Data Bus Buffer Summary

Control Signals R/$\overline{W}$	$\overline{CS}$	Data Bus Buffer State
L	L	Write Mode — Tri-State
H	L	Read Mode — Output Data

TRANSMIT AND RECEIVE DATA REGISTERS

These registers are used as temporary data storage for the DACIA Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.
- Write-only register.

The Receive Data Register is characterized in a similar fashion as follows:

- Bit 0 is the leading bit received.
- Unused data bits are the high order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped off after being used for external parity checking. Parity and all unused high-order bits are "0".
- Read-only register

Figure 4 shows an example of a Parity Mode single transmitted or received data word. In this example, the data word is formatted with 8 data bits, parity, and two stop bits. Figure 4 also shows a single character transmitted or received in Address/Data Mode. In this example, the address or data word is 8 bits, there is no parity bit, and there are two stop bits. The 10th bit (normal parity bit) is an address/data indicator. A 1 means the 8 bits are an address and a 0 means the 8 bits are data.

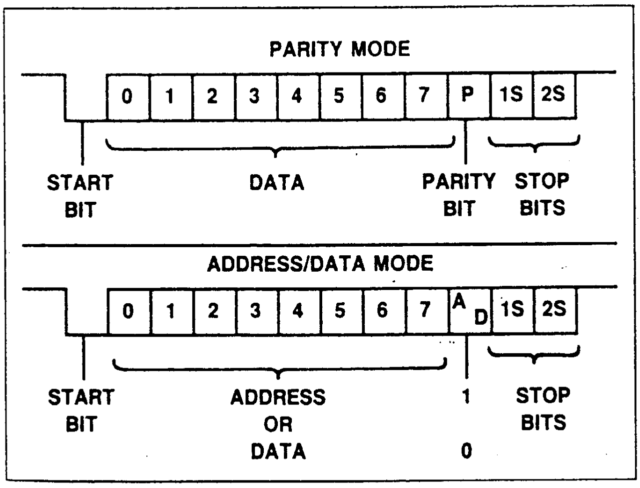


Figure 4. Typical Character

CLOCK CIRCUIT

The internal clock oscillator supplies the time base for the baud rate generator. The oscillator can be driven by a crystal or an external clock, or it can be disabled, in which case the time base for the baud rate is generated by the Receiver External Clock (RxC) and Transmitter External Clock (TxC) input pins. Figure 5 shows the three possible clock configurations.

Crystal (XTALI, XTALO)

These pins are normally connected to an external 3.6864 MHz crystal used as the time base for the baud rate generator. As an alternative, the XTLI pin may be driven with an externally generated clock in which case the XTALO pin must float.

Receiver Clock (RxC)

This pin is the Receiver 16x clock input when the baud rate generator is programmed for external clock. Figure 15 shows timing considerations for RxC.

Transmitter Clock (TxC)

This pin is the transmitter 16x clock input when the baud rate generator is programmed for external clock. Figure 16 shows timing considerations for TxC.

Note

When RxC and TxC are used for external clock input, XTALI must be tied to ground (Vss) and XTALO must be left open (floating).

Clock Out (CLK OUT)

This output is a buffered output from the 3.6864 MHz crystal oscillator. It may be used to drive the XTALI input of another DACIA. This allows multiple DACIA chips to be used in a system with only one crystal needed. CLK OUT is in phase with XTALI.

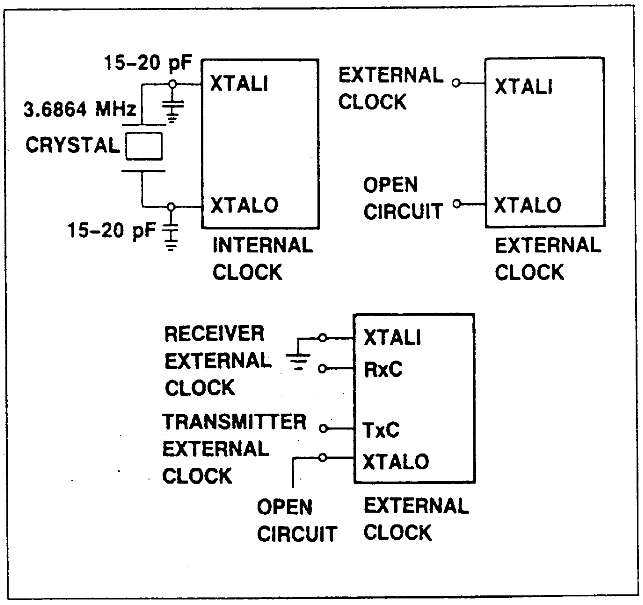


Figure 5. DACIA Clock Generation

CONTROL AND FORMAT REGISTER (CFR)

The Control and Format Register (CFR) is a dual-function, write-only register which allows control of word length, baud rate, control line outputs, parity, echo mode, and compare/TBR access. When the CFR is written to with bit 7 = 0, the CFR functions as a Control Register. When the CFR is written to with bit 7 = 1, the CFR operates as a Formal Register.

Control Register (CFR Addressed with Bit 7 = 0)

7	6	5	4	3	2	1	0
0	TBR/CDR	NO. STOP BITS	ECHO	BAUD RATE SELECTION			

Bit 7 — **Control or Format Register**
0 — Control Register

Bit 6 — **TBR/CDR**
1 — Access the Transmit Break Register (TBR)
0 — Access the Compare Data Register (CDR)

Bit 5 — **Number of Stop Bits Per Character**
1 — Two stop bits
0 — One stop bit

Bit 4 — **Echo Selection (ECHO)**
1 — Echo activated
0 — Echo deactivated

Bits 3-0 — **Baud Rate Selection**

3	2	1	0	Baud Rate
0	0	0	0	50
0	0	0	1	109.2
0	0	1	0	134.58
0	0	1	1	150
0	1	0	0	300
0	1	0	1	600
0	1	1	0	1200
0	1	1	1	1800
1	0	0	0	2400
1	0	0	1	3600
1	0	1	0	4800
1	0	1	1	7200
1	1	0	0	9600
1	1	0	1	19200
1	1	1	0	38400
1	1	1	1	External TxC and RxC Clocks

Format Register (CFR Addressed with Bit 7 = 1)

7	6	5	4	3	2	1	0
1	NUMBER OF DATA BITS		PARITY SELECTION		PARITY ENABLE	$\overline{\text{DTR}}$ CONTROL	$\overline{\text{RTS}}$ CONTROL

Bit 7 — **Control or Format Register**
1 — Format Register

Bits 6-5 — Number of Data Bits Per Character

6	5	No. Bits
0	0	5
0	1	6
1	0	7
1	1	8

Bits 4-3 — Parity Mode Selection

4	3	Selects
0	0	Odd Parity
0	1	Even Parity
1	0	Mark Parity
1	1	Space Parity

Bit 2 — **Parity Enable**
1 — Parity as specified by bits 4-3
0 — No Parity

Bit 1 — **$\overline{\text{DTR}}$ Control**
1 — $\overline{\text{DTR}}$ high
0 — $\overline{\text{DTR}}$ low

Bit 0 — **$\overline{\text{RTS}}$ Control**
1 — $\overline{\text{RTS}}$ high
0 — $\overline{\text{RTS}}$ low

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) is a write-only register that allows each of the possible IRQ sources to be enabled, or disabled, individually without affecting any of the other interrupt enable bits in the register. IRQ sources are enabled by writing to the IER with bit 7 set to a 1 and every bit set to a 1 that corresponds to the IRQ source to be enabled. IRQ sources are disabled by writing to the IER with bit 7 set to a 0 and every bit set to a 1 that corresponds to the IRQ source to be disabled. Any bit (except bit 7) to which a 0 is written is unaffected and remains in its original state. As an example, writing $7F to the IER will disable all IRQ source bits, but writing $FF to the IER will enable all IRQ source bits. A hardware reset ($\overline{\text{RES}}$) clears all IRQ source bits to the 0 state. Bit assignments for the IER are as follows:

7	6	5	4	3	2	1	0
CLEAR/ SET BITS	TDR EMPTY IE	$\overline{\text{CTS}}$ IE	$\overline{\text{DCD}}$ IE	$\overline{\text{DSR}}$ IE	PARITY ERROR IE	FRM OVR BRK CPR IE	RDR FULL IE

INTERRUPT STATUS REGISTER (ISR)

The Interrupt Status Register (ISR) is a read-only register that identifies the current status condition for each DACIA internal IRQ source. Bits 6 through 0 of the ISR are set to a 1 whenever the corresponding IRQ source condition has occurred in the DACIA. Bit 7 identifies if any of the IRQ source status bits have been set in the ISR.

7	6	5	4	3	2	1	0
ANY BIT SET	TDR EMPTY	$\overline{\text{CTS}}$ TRANS	$\overline{\text{DCD}}$ TRANS	$\overline{\text{DSR}}$ TRANS	PARITY ERROR	FRM OVR BRK CPR	RDR FULL

Bit 7 — Any Bit Set
- 1 — Any bit (6 through 0) has been set to a 1
- 0 — No bits have been set to a 1

Bit 6 — Transmit Data Register Empty (TDR EMPTY)
- 1 — Transmit Data Register has been transferred to the shift register
- 0 — New data has been written to the Transmit Data Register

Bit 5 — Transition On $\overline{\text{CTS}}$ Line ($\overline{\text{CTS}}$ TRANS)
- 1 — A positive or negative transition has occurred on $\overline{\text{CTS}}$
- 0 — No transition has occurred on $\overline{\text{CTS}}$, or ISR has been Read

Bit 4 — Transition On $\overline{\text{DCD}}$ Line ($\overline{\text{DCD}}$ TRANS)
- 1 — A positive or negative transition has occurred on $\overline{\text{DCD}}$
- 0 — No transition has occurred on $\overline{\text{DCD}}$, or ISR has been Read

Bit 3 — Transition On $\overline{\text{DSR}}$ Line ($\overline{\text{DSR}}$ TRANS)
- 1 — A positive or negative transition has occurred on $\overline{\text{DSR}}$
- 0 — No transition has occurred on $\overline{\text{DSR}}$, or ISR has been Read

Bit 2 — Parity Error
- 1 — A parity error has occurred in received data
- 0 — No parity error has occurred, or the Receive Data Register (RDR) has been Read

Bit 1 — Frame Error, Overrun or Break (FRM, OVR, BRK, CPR)
- 1 — A framing error, receive overrun, or receive break has occured, or, in Compare Mode
- 0 — No error, overrun, break has occured, RDR has been Read, or not in Compare Mode

Bit 0 — Receive Data Register Full (RDR FULL)
- 1 — Shift register data has been transferred to Receive Data Register
- 0 — Receive Data Register has been Read

CONTROL STATUS REGISTER (CSR)

The Control Status Register (CSR) is a read-only register that provides I/O status and error condition information. The CSR is normally read after an IRQ has occurred to determine the exact cause of the interrupt condition.

7	6	5	4	3	2	1	0
FRAMING ERROR	TRANS UNDR	$\overline{\text{CTS}}$ STATUS	$\overline{\text{DCD}}$ STATUS	$\overline{\text{DSR}}$ STATUS	REC BREAK	$\overline{\text{DTR}}$ STATUS	$\overline{\text{RTS}}$ STATUS

Bit 7 — Framing Error
- 1 — A framing error occurred in receive data
- 0 — No framing error occurred, or the RDR was Read

Bit 6 — Transmitter Underrun (TRANS UNDR)
- 1 — Transmit shift register is empty and TDRE bits in IER and ISR are set
- 0 — A write to the TDR has occurred

Bit 5 — $\overline{\text{CTS}}$ Status
- 1 — A low-to-high transition occurred on $\overline{\text{CTS}}$ line
- 0 — A high-to-low transition occurred on $\overline{\text{CTS}}$ line

Bit 4 — $\overline{\text{DCD}}$ Status
- 1 — A low-to-high transition occurred on $\overline{\text{DCD}}$ line
- 0 — A high-to-low transition occurred on $\overline{\text{DCD}}$ line

Bit 3 — $\overline{\text{DSR}}$ Status
- 1 — A low-to-high transition occurred on $\overline{\text{DSR}}$ line
- 0 — A high-to-low transition occurred on $\overline{\text{DSR}}$ line

Bit 2 — REC Break
- 1 — A Receive Break has occurred
- 0 — No Receive Break occurred, or RDR, was read

Bit 1 — $\overline{\text{DTR}}$ Status
- 1 — A low-to-high transition occurred on $\overline{\text{DTR}}$ line
- 0 — A high-to-low transition occurred on $\overline{\text{DTR}}$ line

Bit 0 — $\overline{\text{RTS}}$ Status
- 1 — A low-to-high transition occurred on $\overline{\text{RTS}}$ line
- 0 — A high-to-low transition occurred on $\overline{\text{RTS}}$ line

TRANSMIT BREAK REGISTER (TBR)

The DACIA has two Transmit Break Registers which are write-only registers. Only two bits of these registers are used; one during the Receive mode to command a Transmit Break and the other to provide for Parity/Address recognition. Writing a 1 to bit 1 of the TBR causes a continuous Break to be transmitted by the ACIA associated with the register. Writing a 0 to this bit allows normal transmission to resume. Writing a 1 to bit 0 of the TBR commands the value of the Parity bit to be sent to the Parity Error bit (bit 2 of the ISR). Writing a 0 to this bit allows normal Parity Error recognition to be in force. When an $\overline{RES}$ is received by the DACIA, both of these bits are reset to 0. The bits format for the TBR are as follows:

7	6	5	4	3	2	1	0
NOT USED						TRANS BRK	PAR/ ADDR

Bits 7-2 **Not used (don't care)**

Bit 1 **Transmit Break (TRANS BRK)**
1 Transmit continuous Break until disabled
0 Resume normal transmission

Bit 0 **Parity/Address Recognition (PAR ADDR)**
1 Send value of parity to ISR bit 2
0 Return to normal Parity Error recognition mode

COMPARE DATA REGISTER

The Compare Data Register (CDR) is a write-only register which can be accessed when CFR bit 6 = 0. By writing a value into the CDR, the DACIA is put in the compare mode. In this mode, setting of the RDRF bit is inhibited and the FRM/OVR/BRK/CPR bit (bit 1) on the ISR is set until a character is received which matches the value in the CDR. The next character is then received and the RDRF bit is set. The receiver will now operate normally until the CDR is again loaded.

SUMMARY OF REGISTERS

Table 3 shows the control and status registers associated with the DACIA in a single summary table. Each of the ACIA's has its own set of these seven registers.

OPERATION

The following paragraphs describe ten modes (or conditions) of operation of the DACIA. The modes described are:

- Continuous Data Transmit
- Continuous Data Receive
- Transmit Underrun Condition
- Effects of CTS on Transmitter
- Effects of Overrun on Receiver
- Echo Mode Timing
- Framing Error
- Transmit Break Character
- Receive Break Character
- Automatic Address Recognition

Table 3. Control and Status Registers Format Summary

REGISTER BIT NUMBERS								REGISTER	$\overline{RES}$
7	6	5	4	3	2	1	0		
CLEAR/SET BITS	TDR EMPTY IE	$\overline{CTS}$ IE	$\overline{DCD}$ IE	$\overline{DSR}$ IE	PARITY ERROR IE	FRM, OVR BRK, CPR IE	RDR FULL IE	INTERRUPT ENABLE REGISTERS	\$80
ANY BIT SET	TDR EMPTY	$\overline{CTS}$ TRANS	$\overline{DCD}$ TRANS	$\overline{DSR}$ TRANS	PARITY ERROR	FRM, OVR BRK, CPR	RDR FULL	INTERRUPT STATUS REGISTERS	—
FRAMING ERROR	TRANS UNDR	$\overline{CTS}$ STATUS	$\overline{DCD}$ STATUS	$\overline{DSR}$ STATUS	REC BREAK	$\overline{DTR}$ STATUS	$\overline{RTS}$ STATUS	STATUS REGISTERS	—
0	TBR/ CDR	NO. STOP BITS	ECHO	BAUD RATE SELECTION				CONTROL REGISTERS AND FORMAT REGISTERS	—
1	NUMBER OF DATA BITS		PARITY SELECTION		PARITY ENABLE	$\overline{DTR}$ CONTROL	$\overline{RTS}$ CONTROL		
NOT USED						TRANS BRK	PAR/ ADDR	TRANSMIT BREAK REGISTERS	\$0F
COMPARE BITS (ADDRESS RECOGNITION)								COMPARE DATA REGISTERS	—

CONTINUOUS DATA TRANSMIT

In the normal operating mode, the TDRE bit in the ISR signals the MPU that the DACIA is ready to accept the next data word. An $\overline{IRQ}$ occurs if the corresponding TDRE IRQ enable bit is set in the IER. The TDRE bit is set at the beginning of the start bit. When the MPU writes a word to the TDR the TDRE bit is cleared. In order to maintain continuous transmission the TDR must be loaded before the stop bit(s) are ended. Figure 6 shows the relationship between $\overline{IRQ}$ and TxD for the Continuous Data Transmit mode.

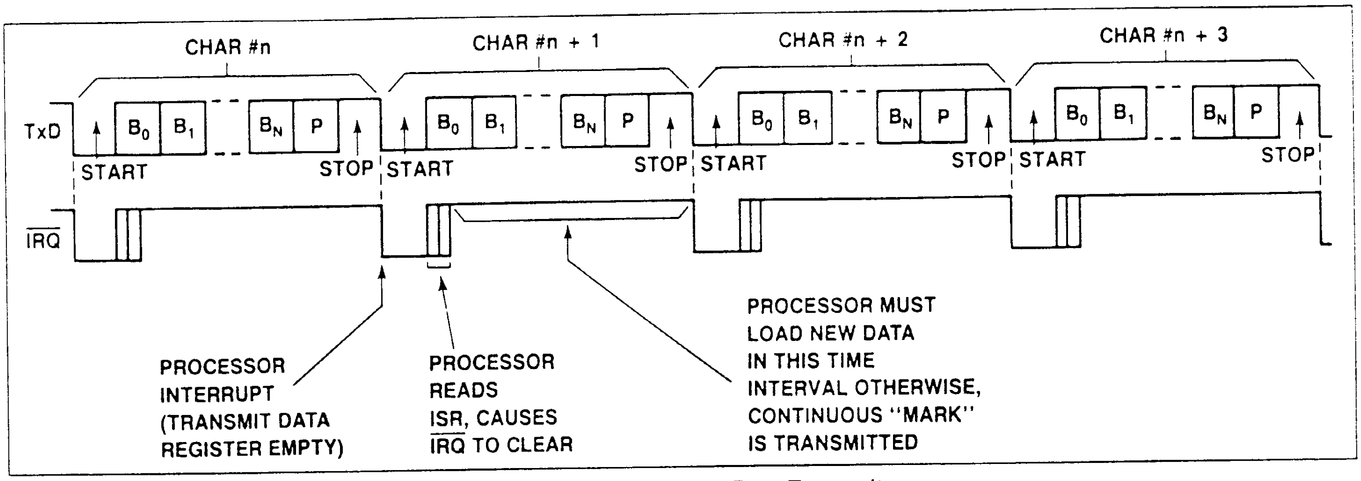


Figure 6. Continuous Data Transmit

CONTINUOUS DATA RECEIVE

Similar to the continuous data transmit mode, the normal receive mode sets the RDRF bit in the ISR when the DACIA has received a full data word. This occurs at about the 9/16 point through the stop bit. The processor must read the RDR before the next stop bit, or an overrun error occurs. Figure 7 shows the relationship between $\overline{IRQ}$ and RxD for the continuous Data Receive mode.

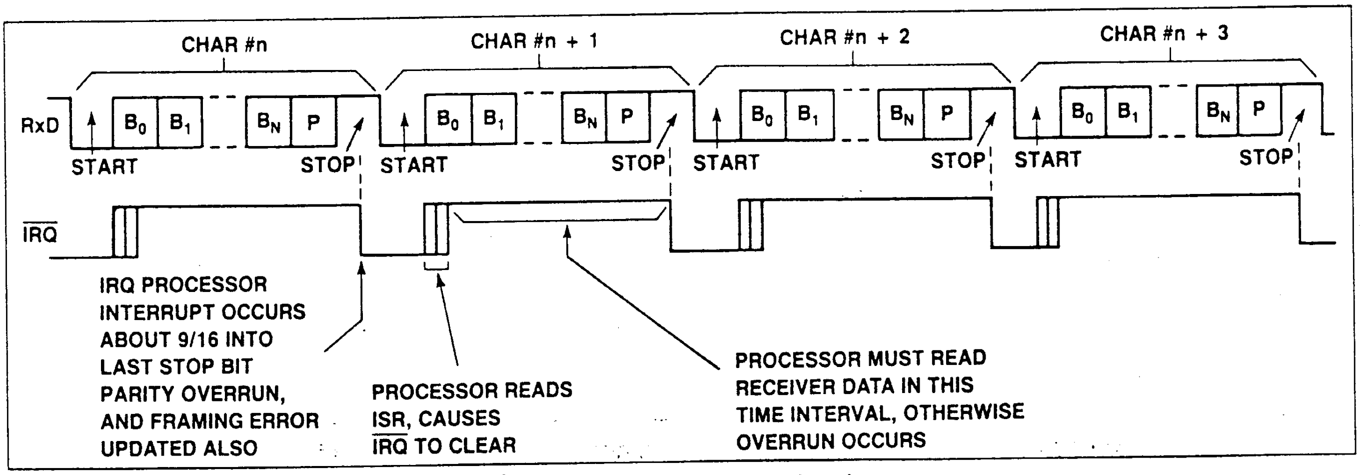


Figure 7. Continuous Data Receive

TRANSMIT UNDERRUN CONDITION

If the MPU is unable to load the TDR before the last stop bit is sent, the TxD line goes to the MARK condition and the underrun flag is set. This condition persists until the TDR is loaded with a new word. Figure 8 shows the relation between $\overline{IRQ}$ and TxD for the Transmit Underrun Condition.

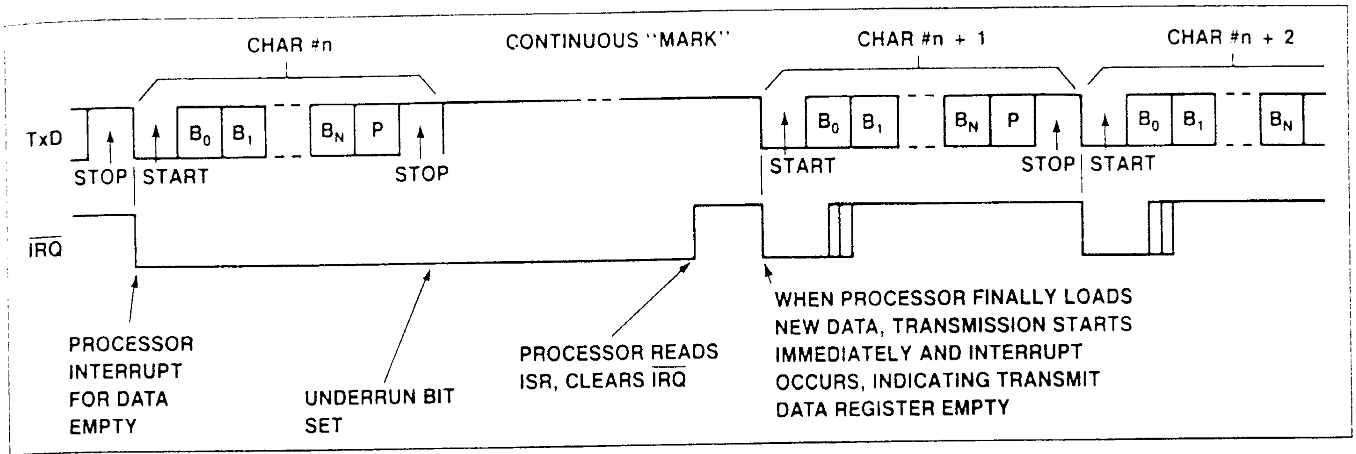


Figure 8. Transmit Underrun Condition Relationship

EFFECTS OF $\overline{CTS}$ ON TRANSMITTER

The $\overline{CTS}$ control line controls the transmission of data or the hand-shaking of data to a "busy" device (such as a printer). When the $\overline{CTS}$ line is low, the transmitter operates normally. Any transition on this line sets the $\overline{CTS}$ bit in the ISR. A high condition inhibits the TDRE bit in the ISR from becoming set. The word currently in the shift register continues to be sent but any word in the TDR is held until $\overline{CTS}$ goes low. At the high-to-low transition the $\overline{CTS}$ bit in the ISR is again set. Figure 9 shows the relationship of $\overline{IRQ}$, TxD, and $\overline{CTS}$ for the effects of $\overline{CTS}$ on the transmitter.

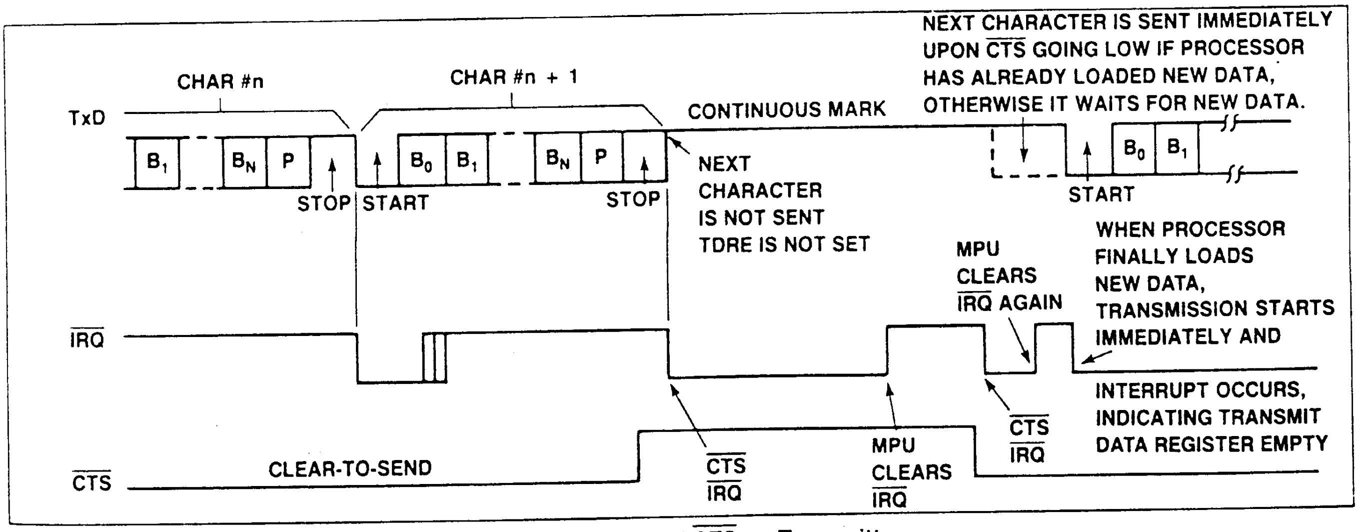


Figure 9. Effects of $\overline{CTS}$ on Transmitter

EFFECTS OF OVERRUN ON RECEIVER

If the processor does not read the RDR before the stop bit of the next word, an overrun error occurs, the overrun bit is set in the ISR, and the new data word is not transferred to the RDR. The RDR contains the last word not read by the MPU and all following data is lost. The receiver will return to normal operation when the RDR is read. Figure 10 shows the relation of $\overline{IRQ}$ and RxD for the effects of overrun on the receiver.

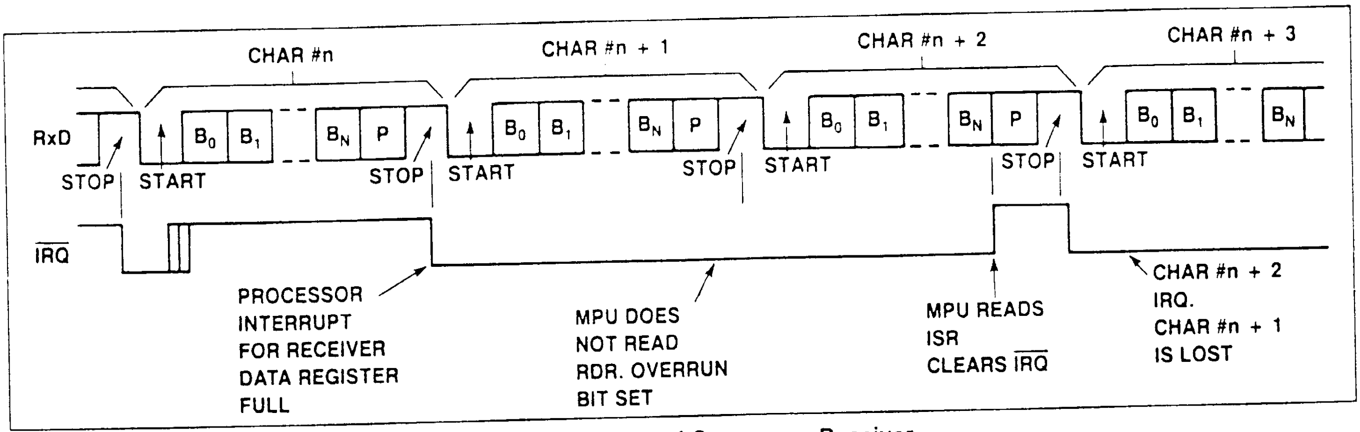


Figure 10. Effects of Overrun on Receiver

ECHO MODE TIMING

In the Echo Mode, the TxD line re-transmits the data received on the RxD line, delayed by 1/2 of a bit time. An internal underrun mode must occur before Echo Mode will start transmitting. In normal transmit mode if TDRE occurs (indicating end of data) an underflow flag would be set and continuous Mark transmitted. If Echo is initiated, the underflow flag will not be set at end of data and continuous Mark will not be transmitted. Figure 11 shows the relationship of RxD and TxD for Echo Mode.

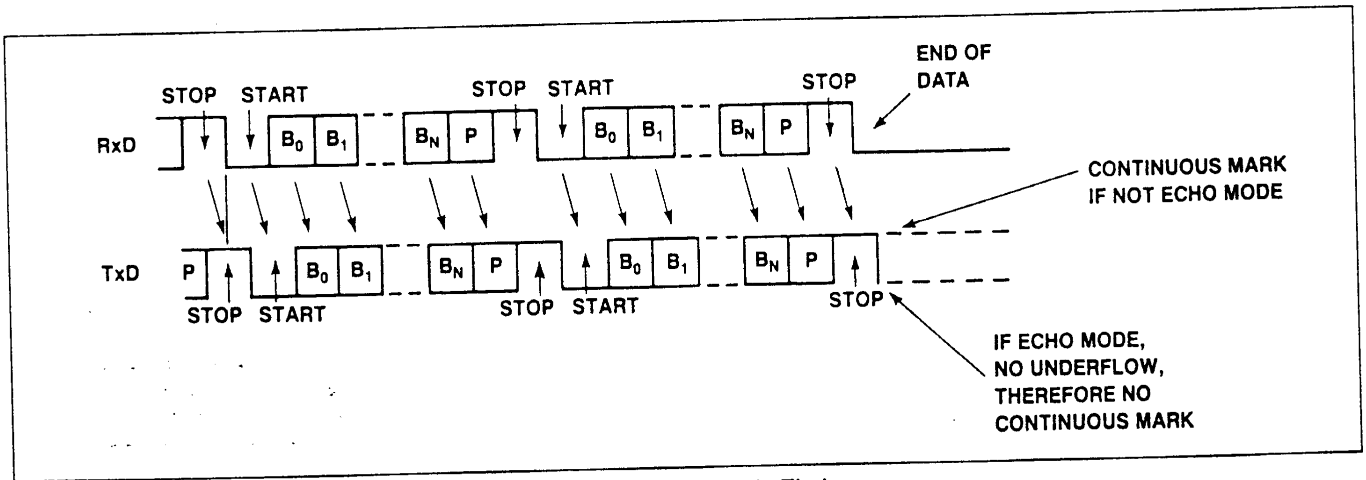


Figure 11. Echo Mode Timing

FRAMING ERROR

Framing error is caused by the absence of stop bit(s) on received data. The framing error bit is set when the RDRF bit is set. Subsequent data words are tested separately, so the status bit always reflects the last data word received. Figure 12 shows the relationship of $\overline{IRQ}$ and RxD when a framing error occurs.

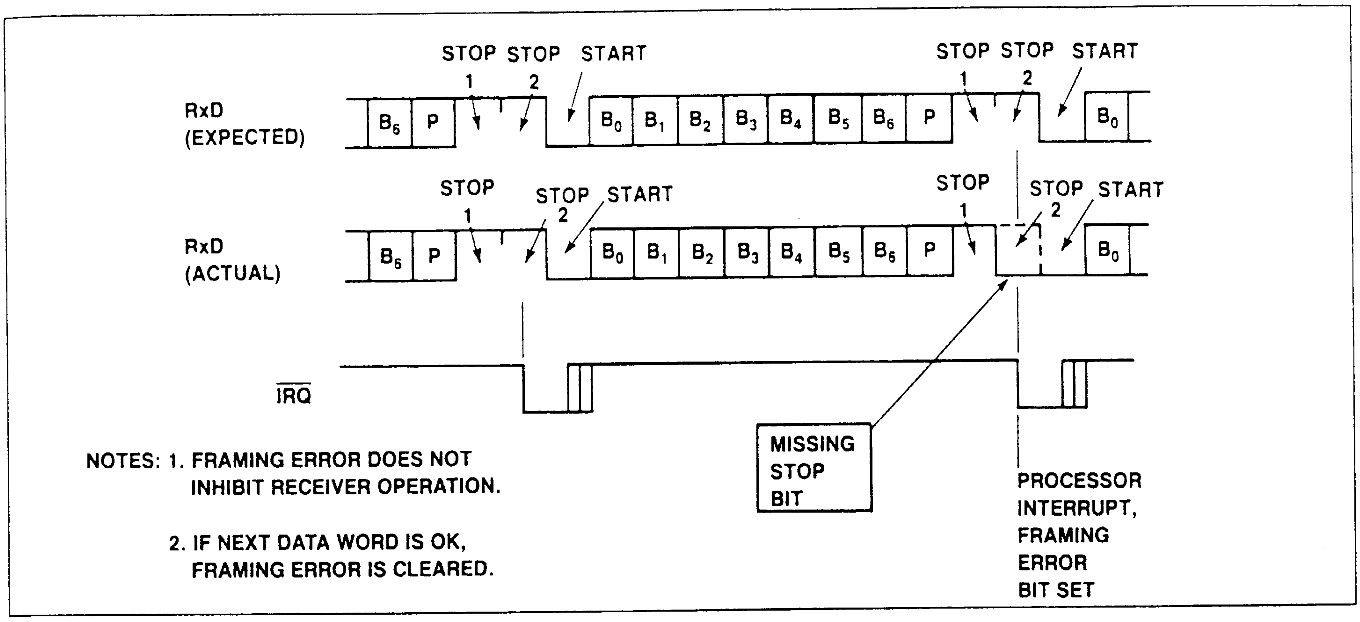


Figure 12. Framing Error

TRANSMIT BREAK CHARACTER

A Break may be transmitted by storing a value of $00 in the IER. After storing zero in the IER the Break is transmitted immediately. Care should be exercised so that a character in transmission is not disturbed inadvertently. The Break level lasts until other than $00 is stored in the IER at which time a stop bit is sent and transmission may resume. At least one full word time of Break will be sent regardless of the length of time between starting and stopping the Break character. Figure 13 shows the relationship of $\overline{IRQ}$ and TxD for a Transmit Break character.

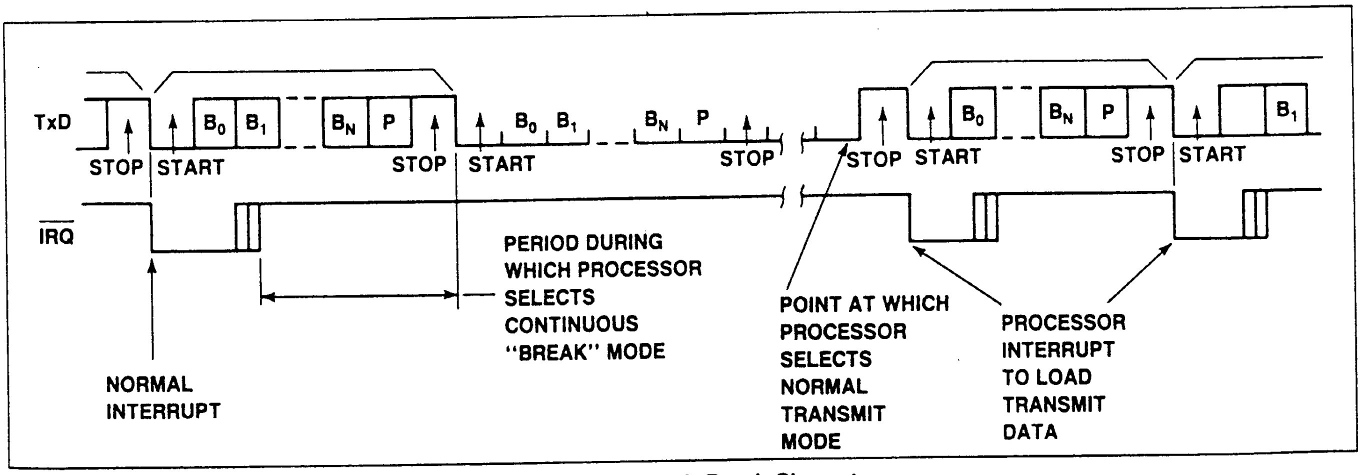


Figure 13. Transmit Break Character

RECEIVE BREAK CHARACTER

In the event that a Break character is received by the receiver, the Break bit is set. The receiver does not set the RDRF bit and remains in this state until a stop bit is received. At this time the next character is to be received normally. Figure 14 shows the relationship of $\overline{IRQ}$ and RxD for a Receive Break Character.

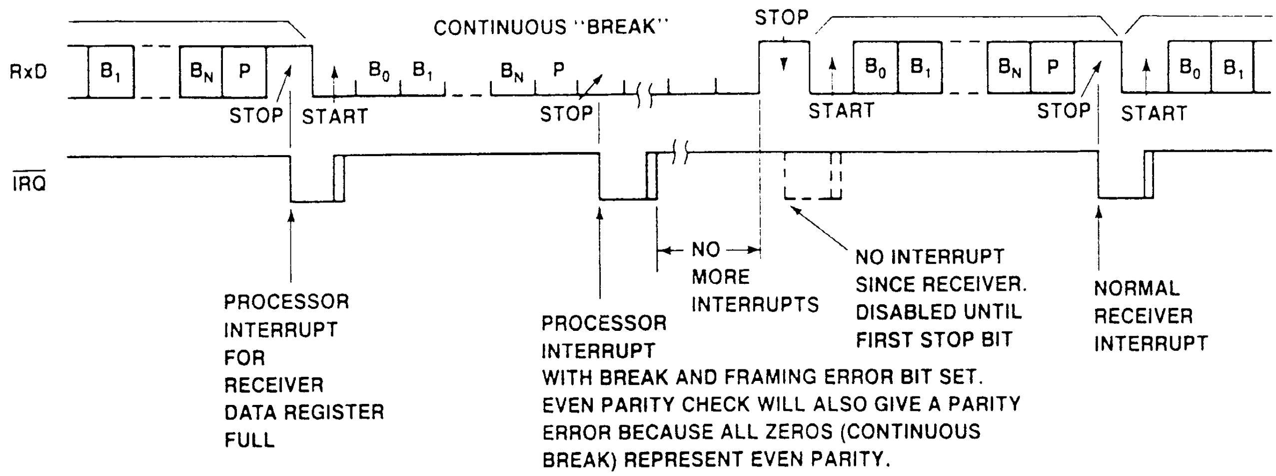


Figure 14. Receive Break Character

AUTOMATIC ADDRESS RECOGNITION

The DACIA offers a unique solution to the standard problem associated with multi-drop environment UARTs and communication interface controllers. In the standard configuration used by other devices, the slave CPU must be constantly interrupted to analyze incoming characters on the communications net to determine if an address word is present and if so, does that address match the address assigned to the slave UART. This CPU interrupt scheme can become intolerable in very large multi-drop networks because every slave on the communications net must "wake-up" it's CPU for every character sent down the network by the master. The end result is that the CPUs on the communications net are constantly being interrupted for the mundane task of address recognition.

To avoid this constant CPU interrupt problem, the DACIA has been designed to do address comparison and recognition internally without the need for CPU intervention. Therefore, the slave CPU is not interrupted until the DACIA has determined that the character sent over the communications net by the master was an address and the address matched the address stored in the DACIA Compare Register. At this point the DACIA interrupts the CPU, goes out of Compare Mode, and receives the string of characters being transmitted by the master, (i.e., the data characters). When all data has been received by the slave, it's CPU must again write the slave address into the DACIA Compare Register which automatically puts it back into the Compare Mode, waiting for another address character.

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the CFR Control Register, as shown in Table 4.

Generating Other Baud Rates

By using a different crystal, other baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the DACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 3) must be the clock input and XTALO (pin 4) must be a nonconnect.

Table 4. Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 3.6864 MHz Crystal	Baud Rate Generated With a Crystal of Frequency (f)
3	2	1	0			
0	0	0	0	73,728	$(3.6864 \times 10^6)/73{,}728 = 50$	f/73,728
0	0	0	1	33,538	$(3.6864 \times 10^6)/33{,}538 = 109.92$	f/33,538
0	0	1	0	27,408	$(3.6864 \times 10^6)/27{,}408 = 134.58$	f/27,408
0	0	1	1	24,576	$(3.6864 \times 10^6)/24{,}576 = 150$	f/24,576
0	1	0	0	12,288	$(3.6864 \times 10^6)/12{,}288 = 300$	f/12,288
0	1	0	1	6,144	$(3.6864 \times 10^6)/6{,}144 = 600$	f/6,144
0	1	1	0	3,072	$(3.6864 \times 10^6)/3{,}072 = 1{,}200$	f/3,072
0	1	1	1	2,048	$(3.6864 \times 10^6)/2{,}048 = 1{,}800$	f/2,048
1	0	0	0	1,536	$(3.6864 \times 10^6)/1{,}536 = 2{,}400$	f/1,536
1	0	0	1	1,024	$(3.6864 \times 10^6)/1{,}024 = 3{,}600$	f/1,024
1	0	1	0	768	$(3.6864 \times 10^6)/768 = 4{,}800$	f/768
1	0	1	1	512	$(3.6864 \times 10^6)/512 = 7{,}200$	f/512
1	1	0	0	384	$(3.6864 \times 10^6)/384 = 9{,}600$	f/384
1	1	0	1	192	$(3.6864 \times 10^6)/192 = 19{,}200$	f/192
1	1	1	0	96	$(3.6864 \times 10^6)/96 = 38{,}400$	f/96
1	1	1	1	16	TxC/16 = Baud Rate or RxC/16 = Baud Rate	

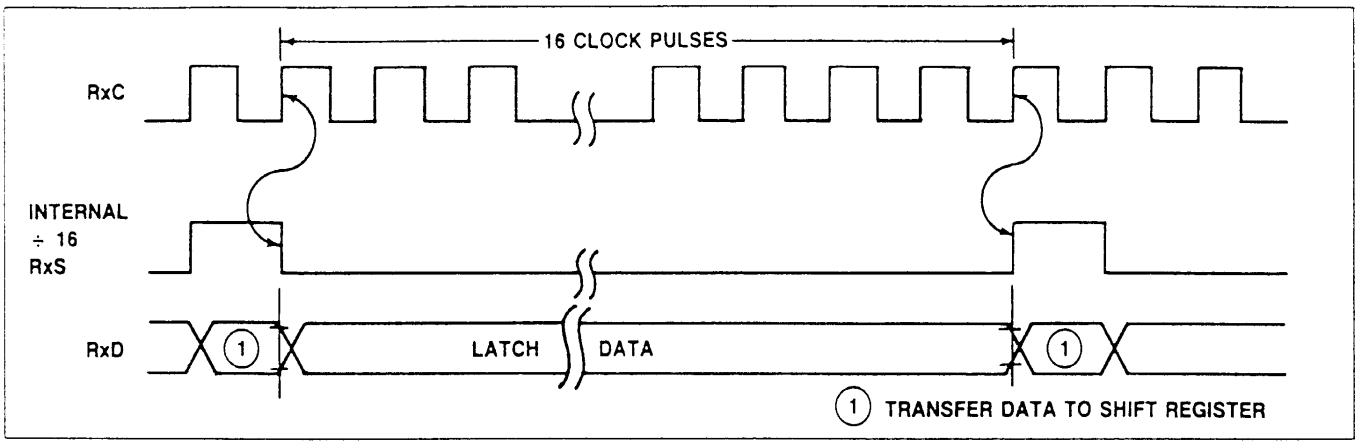


Figure 15. DACIA External Clock Timing — Receive Data

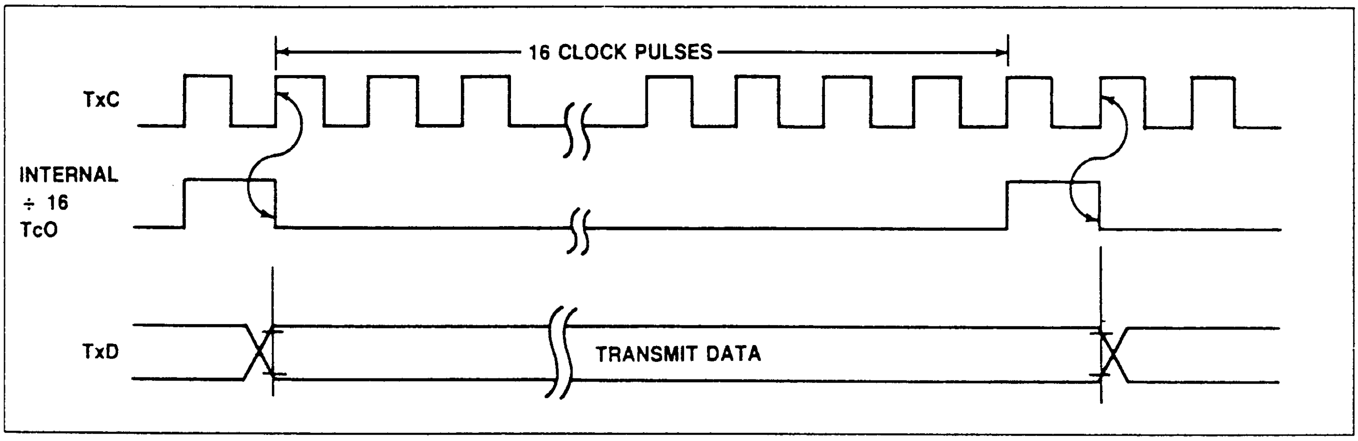


Figure 16. DACIA External Clock Timing — Transmit Data

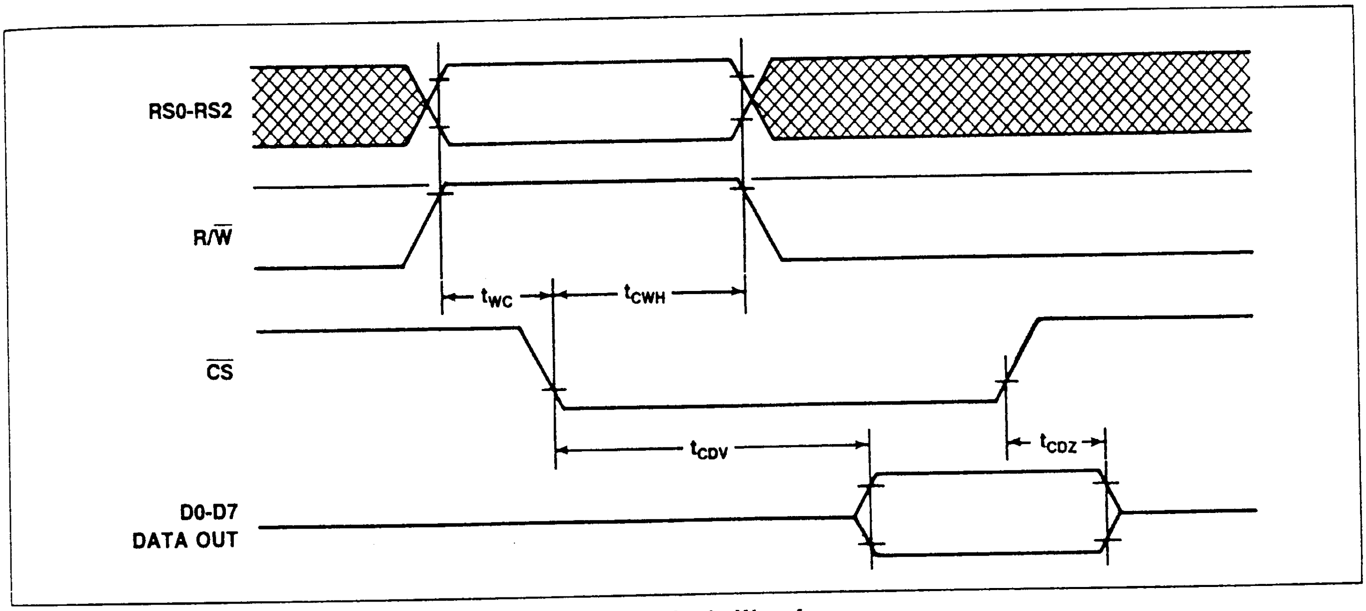
AC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = T_L to T_H)

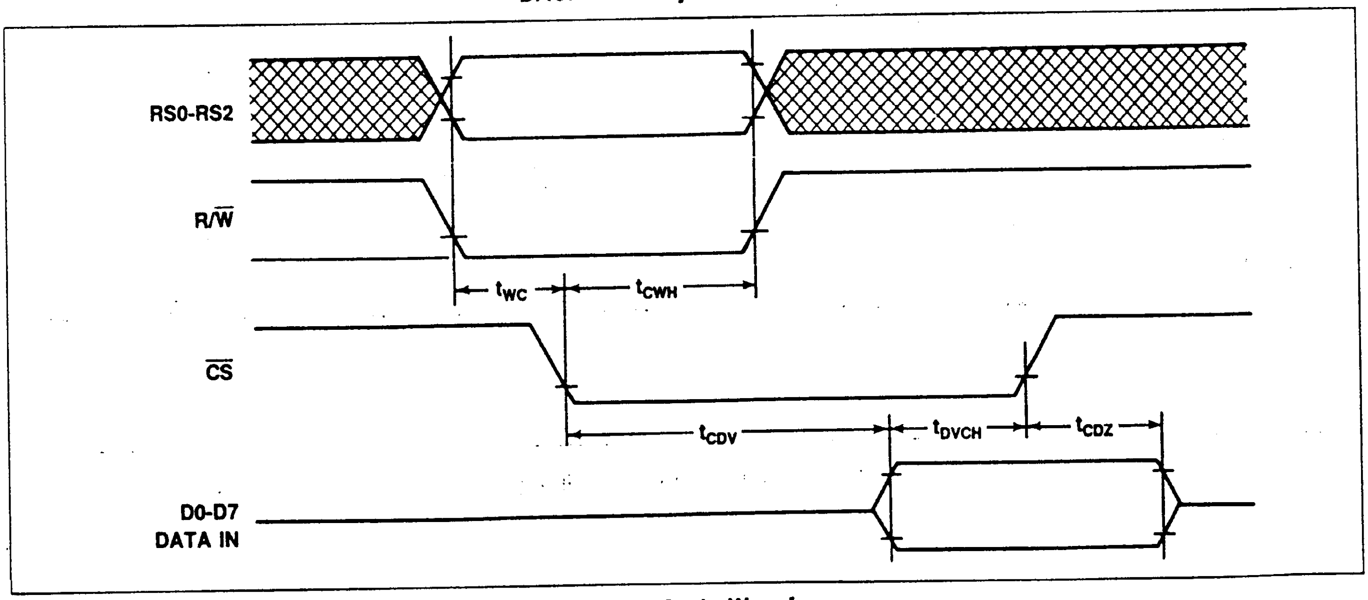
READ/WRITE TIMING

Characteristic	Symbol	2 MHz Min	2 MHz Max	4 MHz Min	4 MHz Max	Unit
R/$\overline{W}$, RS0–RS2 Valid to $\overline{CS}$ Low (Setup Time)	t_{WC}	0	—	0	—	ns
$\overline{CS}$ Low to R/$\overline{W}$, RS0–RS2 (Hold Time)	t_{CWH}	65	—	65	—	ns
$\overline{CS}$ Low to Data Valid	t_{CDV}	—	100	—	100	ns
$\overline{CS}$ High to Data Invalid (Hold Time)	t_{CDZ}	—	10	—	10	ns
Data Valid to $\overline{CS}$ High	t_{DVCH}	20		20		ns

Note:
1. All times are in nanoseconds.



DACIA Read Cycle Waveforms

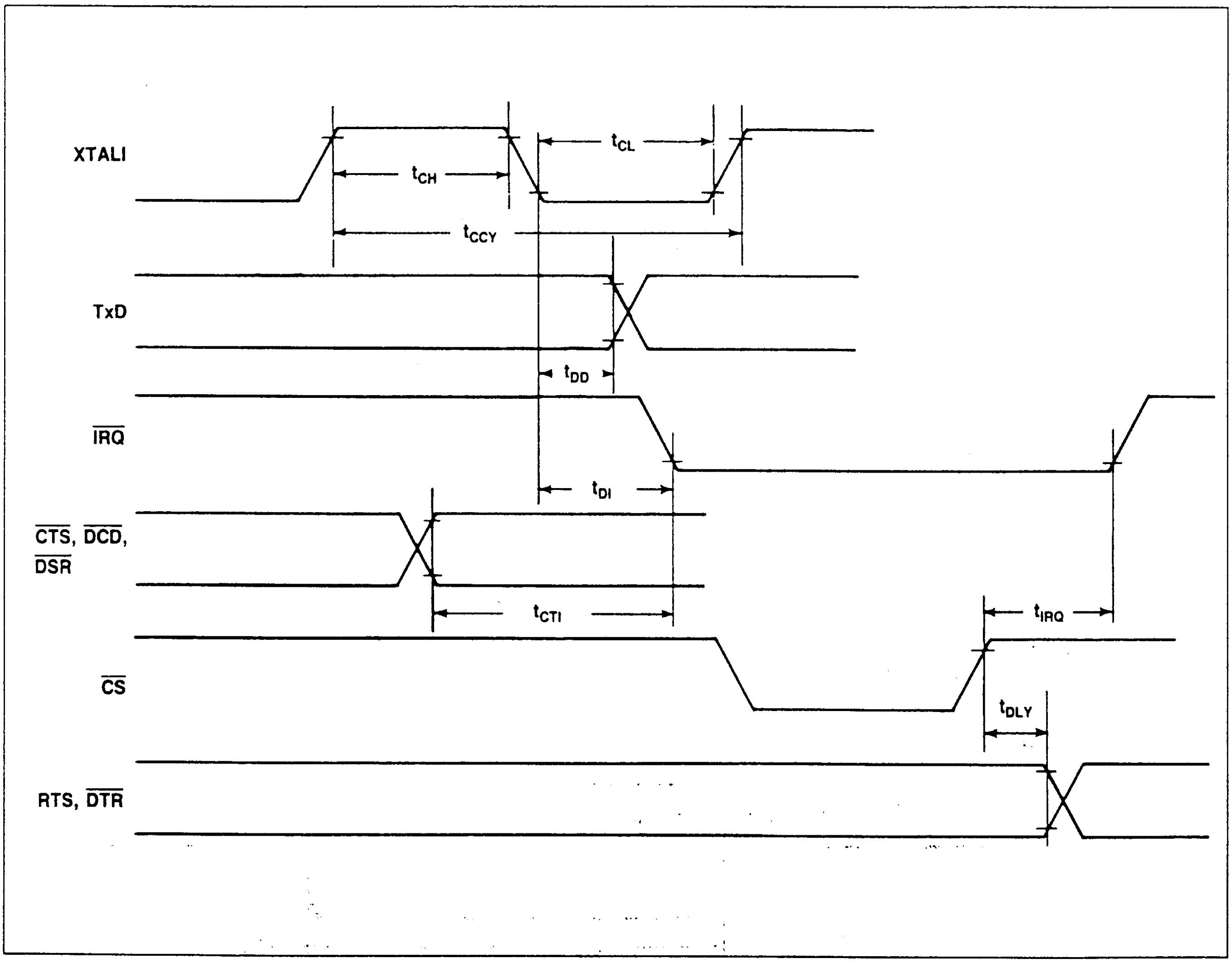


DACIA Write Cycle Waveforms

TRANSMIT/RECEIVE TIMING

Characteristic	Symbol	Min	Max	Unit
Transmit/Receive Clock Rate	t_{CCY}	250	—	ns
Transmit/Receive Clock High Time	t_{CH}	100	—	ns
Transmit/Receive Clock Low Time	t_{CL}	100	—	ns
XTALI to TxD Propagation Delay	t_{DD}	—	250	ns
XTALI to $\overline{IRQ}$ Propagation Delay	t_{DI}	—	250	ns
$\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ to $\overline{IRQ}$	t_{CTI}	—	150	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	150	ns
$\overline{RTS}$, $\overline{DTR}$ Propagation Delay	t_{DLY}	—	150	ns

Note:
1. All times are in nanoseconds.



DACIA Transmit/Receive Timing

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ± 5%
Temperature Range Commercial Industrial	T_A	 0° to 70°C −40°C to +85°C

DC CHARACTERISTICS

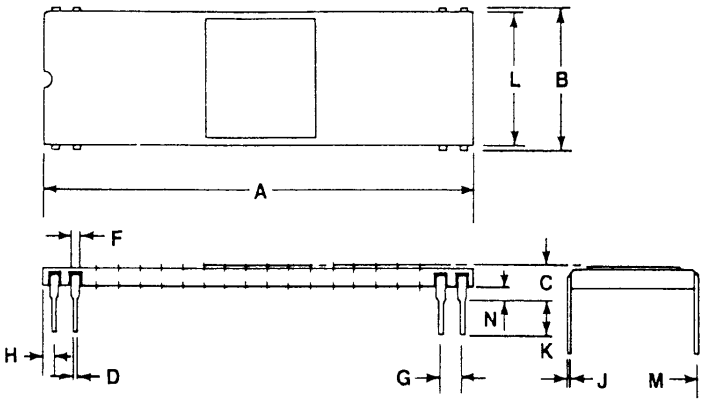
(V_{CC} = 5.0 V ±5%, V_{SS} = 0V, T_A = T_L to T_H, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTALI and XTALO XTALI and XTALO	V_{IH}	 +2.0 +2.4	 — —	 V_{CC} + 0.3 V_{CC} + 0.3	V	
Input Low Voltage Except XTALI and XTALO XTALI and XTALO	V_{IL}	 −0.3 −0.3	 — —	 +0.8 +0.4	V	
Input Leakage Current $R/\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RxD, $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$, $\overline{RxC}$, $\overline{TxC}$, $\overline{CS}$	I_{IN}	—	10	50	μA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7	I_{TSI}	—	±2	10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0–D7, TxD, CLK OUT, RTS, DTR	V_{OH}	+2.4 1.5	— —	— —	V	V_{CC} = 4.75V I_{LOAD} = −100 μA
Output Low Voltage D0–D7, TxD, CLK OUT, RTS, DTR	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output Leakage Current (Off State) $\overline{IRQ}$	I_{OFF}	—	±2	±10	μA	V_{CC} = 5.25V V_{OUT} = 0 to 2.4V
Power Dissipation	P_D	—		10	mW/MHz	
Input Capacitance Except XTALI and XTALO XTALI and XTALO	C_{IN}	 — —	 — —	 5 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

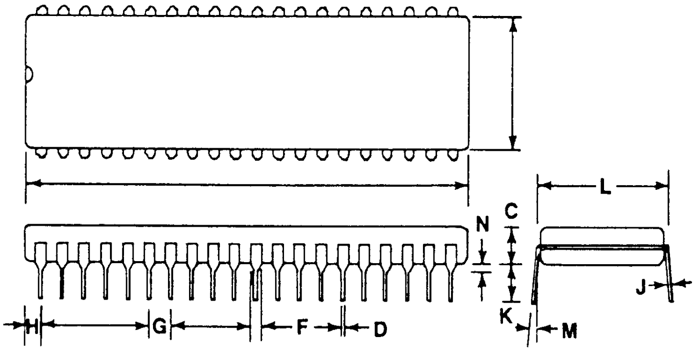
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50 29	51 31	1 980	2.020
B	14 86	15 62	0 585	0 615
C	2 54	4 19	0 100	0 165
D	0 38	0 53	0 015	0 021
F	0.76	1 40	0 030	0 055
G	2.54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15.37	0 575	0 605
M	0°	10°	0°	10°
N	0 51	1 52	0.020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
V	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040