MHS MATRA-HARRIS SEMICONDUCTOR

data sheet

82716/VSDD
VIDEO STORAGE AND DISPLAY DEVICE

ADVANCE INFORMATION

JULY 1986

Features

- OBJECT HANDLING (UP TO 16 OBJECTS)
- BIT MAP AND CHARACTER OBJECTS
- RESOLUTION UP TO 640 x 512 PIXELS
- 16 COLORS FROM A 4096 PALETTE
- ARBITRATION OF PROCESSOR RAM ACCESS
- NAPLP AND CEPT COMPATIBLE
- UP TO 512K BYTES OF DISPLAY MEMORY
- DYNAMIC RAM CONTROL FUNCTIONS
- COMPATIBLE WITH 8 AND 16 BIT MICROPROCESSORS
- TWIN-MODE OPERATION FOR HIGHER THROUGHPUT
- RANGE OF CLOCK RATES
  - 82716 14.5 MHz 5V + / – 10 %
    25 MHz VIDEO CLOCK
  - 82716-3 10.0 MHz 5V + / – 5 %
    15 MHz VIDEO CLOCK

Description

The 82716/VSDD is a high performance VLSI circuit offering advanced display capabilities for Videotex and medium resolution graphics displays. Its internal architecture allows it to be connected to any Intel compatible processor having a multiplexed address and data bus. The screen image is constructed from various "objects" residing in the VSDD memory that are specified by the user. These "objects" may be described as pixels or as characters by way of the RAM based character generators, that are also user-defined. In conjunction with appropriate software the VSDD can be made to be compatible with such video standards as NAPLPS, CGI or user's own custom configurations. The multi-window features and resolution make the VSDD ideal for :

- Mixed Alphanumeric / Graphic Terminals
- Semi Graphic Displays
- Home Information Systems, TVs VCRs Games, Videotex and Home Computers
- Videotex Terminals
- Real-Time Process Control Monitoring Equipment

Figure 1 shows the VSDD block diagram. The VSDD has 3 primary external interfaces : the µp interface, the dynamic RAM display memory interface and the video pixel output.

Through the µp interface the CPU can update the RAM which is divided into register segments and display information. Access to the dynamic RAM is controlled exclusively by the VSDD's DMA controller. The DMA controller accesses display memory and manages the internal line buffers used to build the horizontal scan lines.

The VSDD supports the simultaneous display of information from several sources. Each of these sources is an "object" and is assigned to a display window within the VSDD screen. The VSDD can simultaneously display up to 16 different objects. As the VSDD forms a scan line it gathers information into one of the internal line buffers. While one buffer is being updated with the next scan line, the other buffer is being read out to the color lookup table.

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An object is defined as a list of pixels or characters within the VSDD DRAM memory. Each object is described by an entry in the "Object Descriptor Table" (ODT) that contains positional information, color, size and various other attributes. The effective X-Y coordinates of an object can be changed at any time, without reference to the object itself, thus allowing independent object animation as shown in figure 2.

An object can be replaced by another object by changing the pointer in the ODT, allowing the possibility of many more objects in memory than on display at any one time.

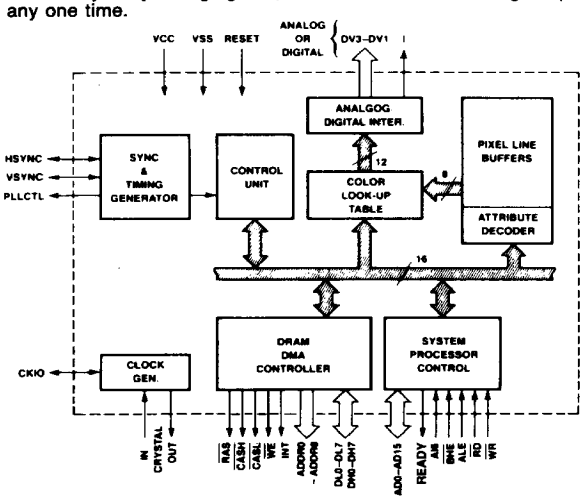


Figure 1 : VSDD Block Diagram

Pin Description

Symbol	Pin	Type	Function
AD0-AD15	60-53 51-44	I/0	Processor system bus multiplexed address and data lines
A16	61	I	High order address input
$\overline{BHE}$	62	I	Byte high enable, active for 16-bit access
ALE	63	I	Address Latch Enable
$\overline{RD}$	64	I	Processor read signal
$\overline{WR}$	65	I	Processor write signal
RESET	4	I	Reset input to initialise VSDD
READY	5	0	Ready output for wait state generation, or free access indicator for MCS-51 family
R/DV3, G/DV2 B/DV1	66-67 68	0	Red, green and blue analog outputs, or high bits of digital output
I/DV0	3	0	Incrustation output, or low digital output
VREF	2	I	Analog voltage reference
HSYNC	7	I/0	As an output supplies horizontal or composite sync. As an input it accepts external horizontal or composite sync
VSYNC	8	I/0	As an output supplies vertical sync. As an input is accepts external vertical sync
DL0-DL7	9-16	I/0	Low order DRAM data bus
DH0-DH7	17 19-25	I/0	High order DRAM data bus
ADDR0-ADDR8	34-26	0	DRAM multiplexed address bus
$\overline{RAS}$	37	0	DRAM Row Address Strobe
$\overline{CASL}$	38	0	Low order Column Address Strobe
$\overline{CASH}$	39	0	High order Column Address Strobe
$\overline{WE}$	36	0	DRAM write signal
CTO	40	0	Construction Time Overflow
XTALIN	41	I	Oscillator input or crystal terminal
XTALOUT	42	0	Oscillator output or crystal terminal
CKIO	43	I/0	As an input receives the external dot clock. As an output, serves as a buffered dot clock
PLLCTL	6	0	PLL control used to fine tune the output
VCC1, VCC2	1-35	I	5 Volt power supply
VSS1, VSS2	52-18	I	Digital ground

Electrical characteristics

ABSOLUTE MAXIMUM RATINGS *

Ambient Temperature Under Bias ..... 0 to 70°C
Storage Temperature ..... – 65°C to 150°C
Voltage From Any Pin with Respect to VSS ..... – 1.0 to 7.0V
Power Dissipation ..... 3 W

** NOTICE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0 to 70°C, VCC1/VCC2 = + 5V +/– 10 %)

Symbol	Parameter	Min	Max	Unit	Test conditions
VREF	Reference Voltage	1.0	2.0	V	Typ = 1.6 V
RVREF	Source Impedance of VREF		200	ohm	
VOH	Output High Voltage	2.4		V	IOH = – 400 µA
VOL	Output Low Voltage		0.4	V	IOL = 2.0 mA
VIH	Input High Voltage	2.0	VCC + 0.5		
VIL	Input Low Voltage	– 0.5	0.8	V	
VIHC	Input High Voltage CKIO and XTALIN	3.5	VCC + 0.5	V	
VILC	Input Low Voltage CKIO and XTALIN	– 0.5	0.8	V	
ILI	Input Leakage Current		+/– 10	µA	0 < Vin < VCC
ILO	Output Leakage Current		+/– 10	µA	0.45 < Vin < Vcc
ICC	Power Supply Current		350	mA	TA = 25°C
CIN	Capacitance of Inputs		10	pF	fc = 1 MHz
CIO	Capacitance of I/O's		15	pF	fc = 1 MHz
COUT	Capacitance of Outputs		10	pF	fc = 1 MHz
COUT	Capacitance of Outputs $\overline{RAS}$, $\overline{CASL}$, $\overline{CASH}$, $\overline{WE}$, CT0		15	pF	fc = 1 MHz
COUT	Capacitance of Outputs R/DV3, G/DV2, B/DV1, I/DV0		7	pF	fc = 1 MHz
CRAS	$\overline{RAS}$ load		200	pF	
CCAS	$\overline{CASL}$, $\overline{CASH}$ loads		100	pF	
$\overline{CWE}$	$\overline{WE}$ load		200	pF	
CCT0	CT0 load		100	pF	
CDij	DL0-DL7 DH0-DH7 loads		100	pF	
CADD	ADDR0-ADDR8 loads		150	pF	

A.C. CHARACTERISTICS (T_A = 0 to 70°C)

RANGE OF CLOCK RATES
82716 : 14.5 MHz VCC = 5V +/− 10 %
82716-3 : 10.0 MHz VCC = 5V +/− 5 %

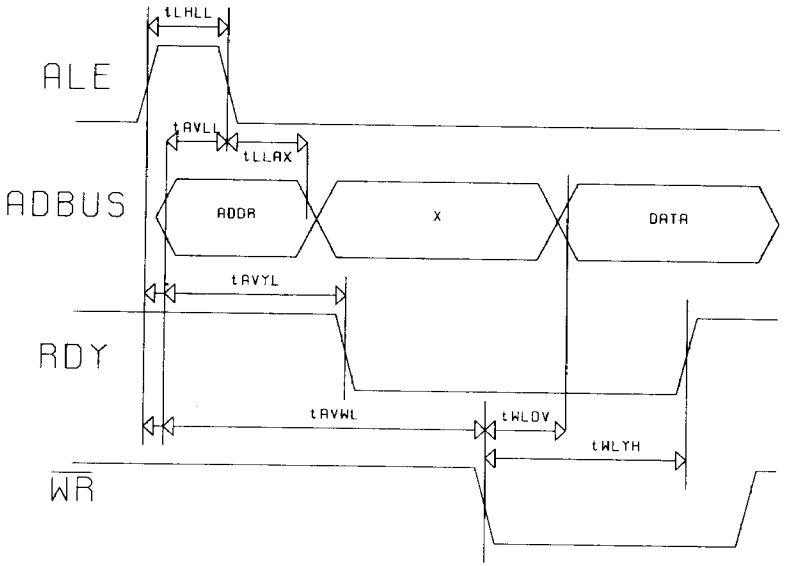
TIMING REQUIREMENTS

Symbol	Parameter	82716		82716-3		Unit	Test conditions
		Min	Max	Min	Max		
tCLCL	CLOCK cycle period	69	200	100	200	ns	
dCCK	Duty cycle	40	60	50	50	%	
tVCLCL	VIDEO CLOCK cycle period	40	100	65	200	ns	
dCVCK	Duty cycle	40	60	50	50	%	
tVCILIH	VIDEO CLOCK rise time		10		10	ns	From 1.0 to 3.5V
tVCIHIL	VIDEO CLOCK fall time		10		10	ns	From 3.5 to 1.0V
tILIH	Input rise time		20		20	ns	From 0.8 to 2.0V
tIHIL	Input fall time		20		20	ns	From 2.0 to 0.8V

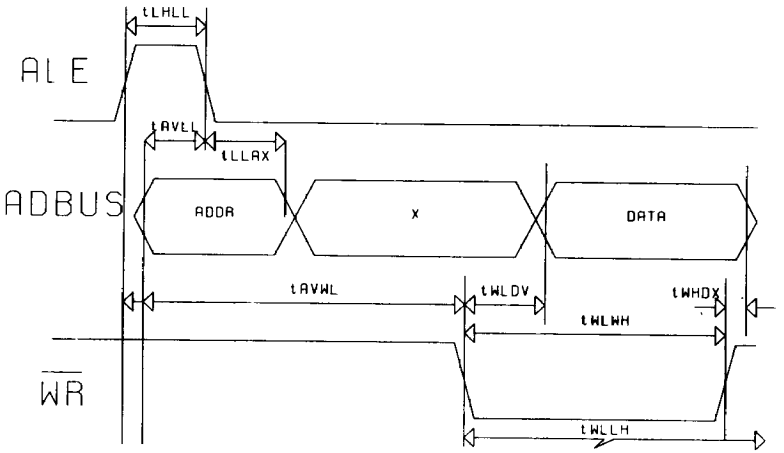
BUS INTERFACE UNIT

CPU WRITE CYCLE TIMINGS

Symbol	Parameter	Min	Max	Unit
tLHLL	ALE pulse width	35		ns
tAVLL	Address set-up time	20		ns
tLLAX	Address Hold Time	5		ns
tAVWL	Address Valid or ALE high (whichever is later) to WR low	75		ns
tAVYL	Address valid or ALE high (wichever is later) to RDY low		90	ns
tWLDV	Data valid after WR low		8tCLCL − 40	ns
tWLYH	WR low to RDY high		14tCLCL + 100	ns
tWLWH	WR pulse width	2tCLCL + 20		ns
tWHDX	Data hold time after WR high	0		ns
tWLLH	WR low to ALE high of next RD/WR cycle	18tCLCL + 100		ns



CPU WRITE CYCLE USING READY TO GENERATE WAIT STATES



CPU WRITE CYCLE NOT USING READY

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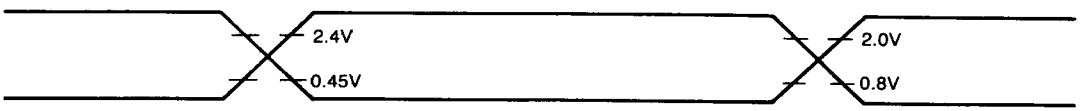
A.C. TESTING INPUT/OUTPUT WAVEFORMS

A.C. inputs during testing are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

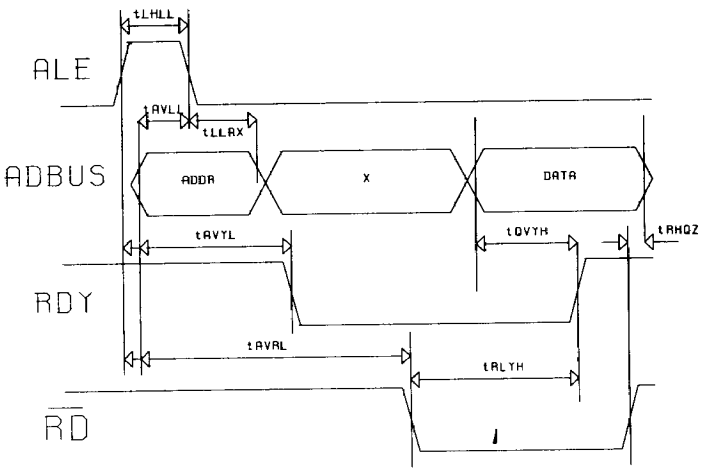


BUS INTERFACE UNIT

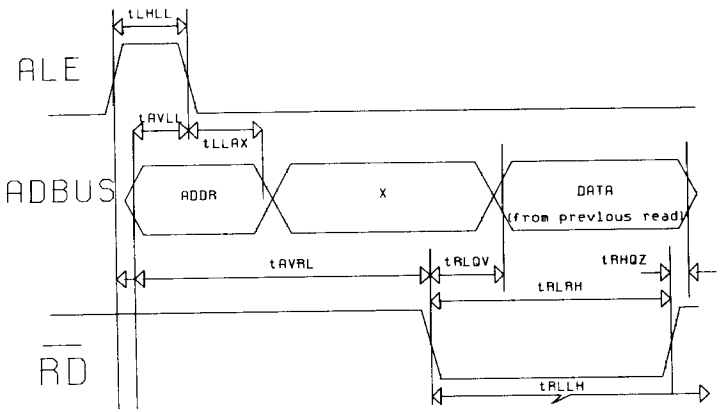
CPU READ CYCLE TIMINGS

Symbol	Parameter	Min	Max	Unit
tRLYH	RD low to RDY high		19tCLCL + 100	ns
tQVYH	Data valid to RDY high	0		ns
tRHQZ	Data float time after RD		40	ns
tRLQV	RD Low to data valid (PRE = 1)	10	40	ns
tRLRH	RD pulse width (PRE = 1)	2tCLCL + 20		ns
tRLLH	RD low to ALE high of next RD/WR cycle	18tCLCL + 100		ns
tAVRL	Address valid or ALE high (wichever is later) to RD low	75		ns

WAVEFORMS



CPU read cycle using ready to generate wait states (PRE = 0)



CPU read cycle not using ready (PRE = 1)

DRAM CONTROLLER

PAGE MODE

		XTAL = 14.5 MHz			Variable clock 5 to 14.5 MHz	
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Slow access**	**Fast access**
tPC	Page Mode Read Cycle	207		ns	3 tCLCL	2 tCLCL
tCP	CAS Precharge Time	64		ns	tCLCL – 5	tCLCL – 5
tCAS	CAS Pulse Width	133		ns	2 tCLCL – 5	tCLCL – 5
tRPM	RAS Pulse Width		6619	ns	96 tCLCL – 5 *	65 tCLCL – 5 *

* Page mode accesses are made in bursts of 32 CAS-only reads the address crosses a column boundary or the accesses are interrupted by the system processor

DRAM CONTROLLER

READ CYCLE

		XTAL = 14.5 MHz(1)			Variable clock 5 to 14.5 MHz	
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Slow access**	**Fast access**
tRC	Random Read Cycle Time	345		ns	5 tCLCL	4 tCLCL
tREF	Refresh time (*) 128 cycles 256 cycles	 2 4		 ms ms	(128/12 * scan line time) + 10 000 tCLCL	
tRP	RAS Precharge Time	133		ns	2 tCLCL – 5	2 tCLCL – 5
tCPN	CAS Precharge Time (non page mode)	202		ns	3 tCLCL – 5	3 tCLCL – 5
tRCD	RAS to CAS Delay Time	64		ns	tCLCL – 5	tCLCL – 5
tRSH	RAS Hold Time	133		ns	2 tCLCL – 5	tCLCL – 5
tCSH	CAS Hold Time	202		ns	3 tCLCL – 5	2 tCLCL – 5
tASR	Row Address Set-Up Time	25		ns	tCLCH – 10	tCLCH – 10
tRAH	Row Address Hold Time	21		ns	tCLCH – 14	tCLCH – 14
tASC	Column Address Set-Up Time	25		ns	tCLCH – 10	tCLCH – 10
tCAH	Column Address Hold Time	177		ns	3 tCLCL – 30	2 tCLCL – 30
tAR	Column Address Hold to RAS	232		ns	3 tCLCL + tCHCL – 10	2 tCLCL + tCHCL – 10
tRAS	RAS Pulse Width	202	20000 (2)	ns	3 tCLCL – 5	2 tCLCL – 5
tCAS	CAS Pulse Width	133	20000 (2)	ns	2 tCLCL – 5	tCLCL – 5
tCRP	CAS to RAS Precharge Time	133		ns	2 tCLCL – 5	2 tCLCL – 5
tQS	Read Data Stable after CAS		118	ns	2 tCLCL – 20	tCLCL – 20

* 12 rows are updated during each scan line.
(1) The figures at 14.5 MHz are given for SAB = 1 (Slow Access) and Duty cycle = 50 %.
For other values of frequency or for fast access, replace the min. or max. value (whichever is applicable) by the formules given in the columns on the right part of the tables.
(2) Independant of frequency and of SAB value.

DRAM CONTROLLER

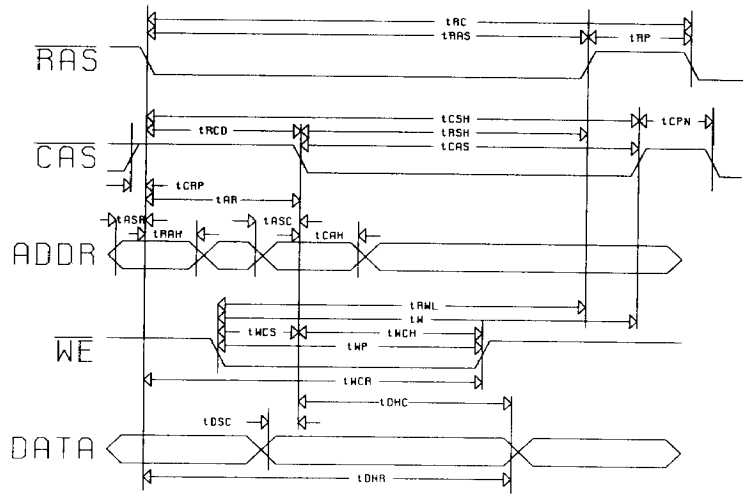
WRITE CYCLE

		XTAL = 14.5 MHz(1)			Variable clock 5 to 14.5 MHz	
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Slow access**	**Fast access**
tRC	Random Write Cycle Time	345		ns	5 tCLCL	4 tCLCL
tRAS	RAS Pulse Width	202	20000 (2)	ns	3 tCLCL – 5	2 tCLCL – 5
tCAS	CAS Pulse Width	133	20000 (2)	ns	2 tCLCL – 5	tCLCL – 5
tWP	Write Command Pulse Width	202		ns	3 tCLCL – 5	2 tCLCL – 5
tWCS	Write Command Set-Up Time	35		ns	tCLCH	tCLCH
tWCH	Write Command Hold Time to CAS	133		ns	2 tCLCL + tCHCL – 40	tCLCL + tCHCL – 40
tWCR	Write Command Hold Time to RAS	202		ns	3 tCLCL + tCHCL – 40	2 tCLCL + tCHCL – 40
tRWL	Write to RAS Lead Time	163		ns	2 tCLCL + tCLCH – 10	tCLCL + tCLCH – 10
tCWL	Write to CAS Lead Time	163		ns	2 tCLCL + tCLCH – 10	tCLCL + tCLCH – 10
tDSC	Data Set-Up Time to CAS	84		ns	tCLCL + tCLCH – 20	tCLCL + tCLCH – 20
tDHC	Data Hold Time after CAS	153		ns	2 tCLCL + tCHCL – 20	tCLCL + tCHCL – 20
tDHR	Data Hold Time after RAS	222		ns	3 tCLCL + tCHCL – 20	2 tCLCL + tCHCL – 20
tR, tF	Rise, Fall Time RAS, CAS	5	40	ns		

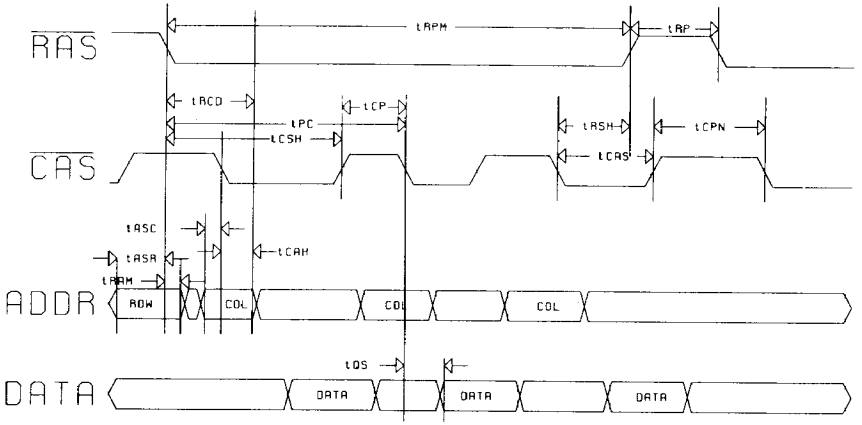
(1) The figures at 14.5 MHz are given for SAB = 1 (Slow Access) and Duty cycle = 50 %.
For other values of frequency or for fast access, replace the min. or max. value (whichever is applicable) by the formules given in the columns on the right part of the tables.
(2) Independant of frequency and of SAB value.

WAVEFORMS

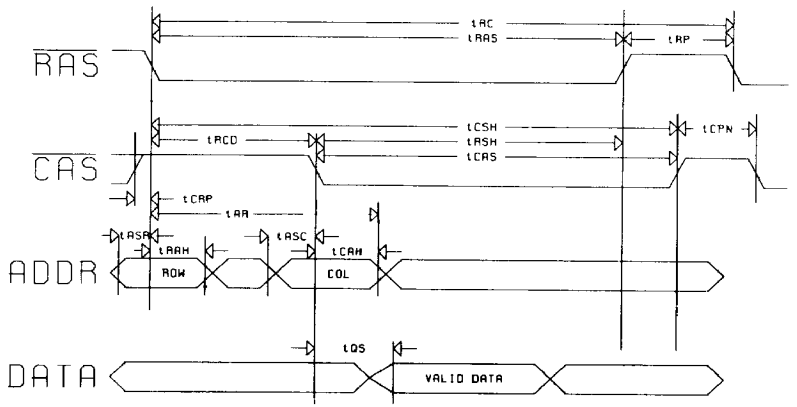
WRITE CYCLE



PAGE MODE READ CYCLE



READ CYCLE



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VIDEO OUTPUT TIMINGS

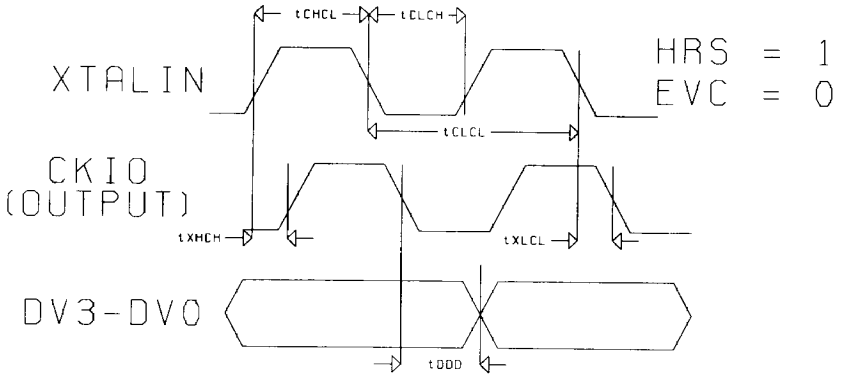
Symbol	Parameter	Min	Max	Unit	Comments
tXHCH	XTALIN high to CKIO high		60	ns	EVC = 0 HRS = 1
tXLCL	XTALIN low to CKIO low		70	ns	EVC = 0 HRS = 1
			75	ns	EVC = 0 HRS = 0
tXLCH	XTALIN low to CKIO high		80	ns	EVC = 0 HRS = 0
tDDD	Digital Data Delay		30	ns	EVC = 0 HRS = 0
			35	ns	EVC = 0 HRS = 1
			55	ns	EVC = 1 HRS = 1
tXHL	XTALIN low to HSYNC low		tCLCH + 150	ns	
tXVL	XTALIN low to VSYNC low		150	ns	

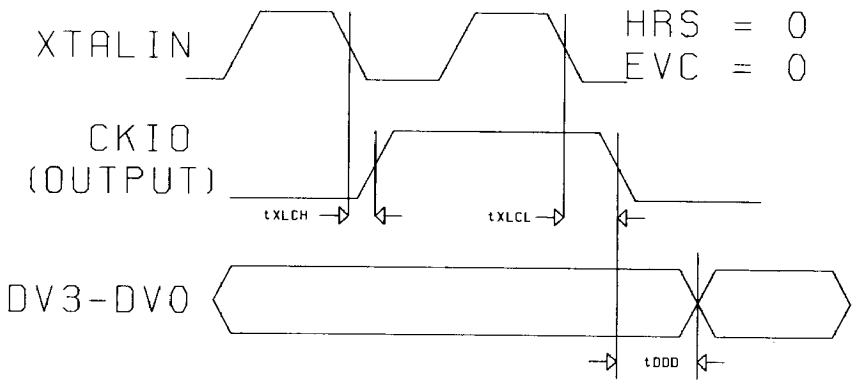
DIGITAL - ANALOG CONVERTER OUTPUT

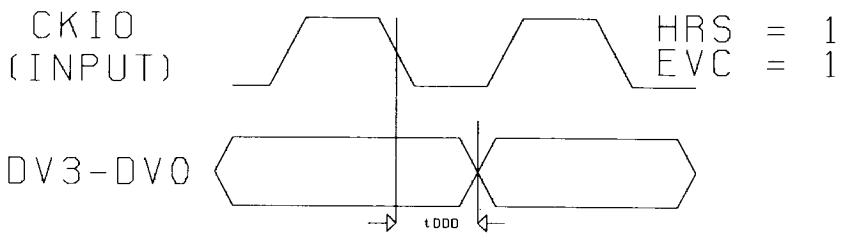
All measurements made with VREF = 1.6V

Symbol	Parameter	Min	Max	Unit	Comments
SLEW	DAC Slew Rate	50		V/µS	VREF = 1.6V
V0	Analog output, code 0	0.25	0.35	V	VREF = 1.6V
VF	Analog output, full scale	1.0	1.2	V	VREF = 1.6V
NLIN	DAC Non - Linearity		+/– 0.5	lsb	lsb (VF - V0) / 15

WAVEFORMS







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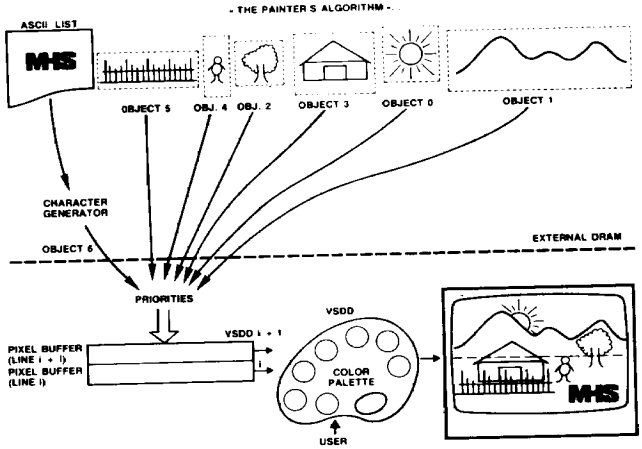


Fig. 2 : Building an animation scene.

MICROPROCESSOR INTERFACE

The VSDD supports both 8 and 16 bit microprocessors from all Intel compatible families using multiplexed address/data buses. VSDD accepts the multiplexed bus signals together with ALE and the read/write commands RD and WR. For 16 bit accesses the byte high enable (BHE) signal is also used. This allows the VSDD to distinguish between byte and word accesses. If the processor request cannot be serviced immediately then the VSDD generates a ready signal (RDY) to extend the processor cycle. In addition to the necessary control signals the interface consists of an address bus of 17 bits (128K byte maximum address space). The VSDD, via bank selection, enables the processor to access up to 512K bytes of display RAM.

Arbitration of display memory is carried out internally by the VSDD, with the processor normally having priority over the VSDD. Accesses made by the system processor through the VSDD to the external DRAM display memory can have an impact on the VSDD's capability to complete the scan line building process. To avoid this the VSDD allows the capability to program the number of priority system processor accesses.

For each frame the user is able to specify the number of high priority accesses (N less than 16) that the system processor may have during the line building process. Thus, N accesses from the system processor will be serviced with a minimum delay by the VSDD concurrently with building the line buffer. The (N + 1) th access will be delayed by wait states (RDY) until the completion of the line buffer. Whenever the VSDD isn't constructing a horizontal line, system processor accesses will be serviced with minimum delay.

For the MCS-51 family the interface is slightly different. This family has no RDY input and cannot be temporarily halted during a memory access. In this case the RDY output is programmed as a "Free Access" indicator. The 8051 can test this bit to see if the VSDD is using the memory, and if not, gain access immediately. Because the 8051 has no RDY input all read operations on VSDD memory must be pipelined. That is to say a dummy read must be performed to set up the address followed by the data transfer on the next read cycle. This means that addresses and data are always out of phase for read operations, the address for the current byte having been provided by the previous read access.

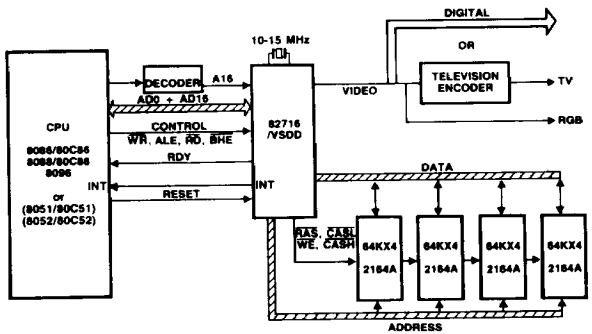


Fig. 3 : Sample System Configuration.

MEMORY MAPPING

The VSDD will support up to 512K bytes of DRAM, organised as 256K x 16 bits. This memory is divided into four 64K x 16 bit banks. The ability to address large amounts of memory enables the VSDD to access several screens or have very large page that can be scrolled in X or Y directions.

Since the processor can only access up to 128K bytes (17 address pins), the VSDD supports windowing of the processor memory into blocks of the VSDD memory by address translation. VSDD memory is separated into a data segment (which contains pixel or character data, character generators, Access Tables and Object Descriptor Tables), and a register segment used to store the screen constants. The processor accesses these two segments by defining a set of base addresses and a window size, in the register segment.

The data and register segment windows in the processor address space are relocatable, while only the data segment in the DRAM address is relocatable. The register segment is fixed at starting location 00000H. The length of the data window can be specified from 4K to 64K bytes while the register segment is fixed at 32 bytes.

VIDEO/DIGITAL OUTPUT

The VSDD has an on-board color look-up table which contains 16 entries defined by 12 bits (4 red, 4 green and 4 blue), for a possible palette of 4096 colors. These colors are addressed by the output of the pixel buffer and fed to three on-board Digital-Analog Converters (DACs). This table may be reinitialised for every frame.

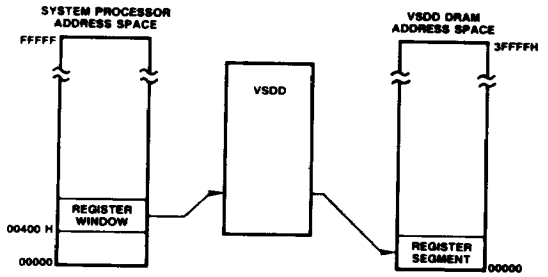
In some applications it is necessary to overlay external video signals. To support this the VSDD has an "Incrustation" pin (I) which can be used as a fast switch signal to allow the display of external video instead of the VSDD output. The Incrustation pin is set by the 111H color code. If Incrustation is to be used a color look-up table entry must contain 111H. The location of the screen to be overlayed is set up to be displayed with a 111H color code. When this color is displayed the I pin is set and user defined logic is triggered to switch in external video.

A digital output mode is also available. In this mode the RGB and I pins provide direct digital output from the pixel buffer by bypassing the color look-up table and the DACs. The data is available as 4-bit words and can be directly connected to a monitor or be further decoded in systems that use data compression techniques such as Alpha-Photographic Videotex.

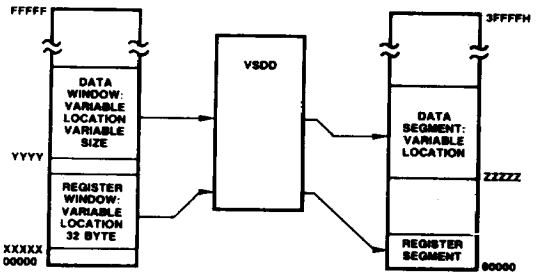
REGISTER SEGMENT

The register segment consists of 16 words (32 bytes) of external memory stored in DRAM, which is read by the VSDD at the end of every frame. These registers contain the basic information for screen constants, DRAM organisation, timing and data segment base addresses. The first location of the register segment is at the physical memory address 00000H in the VSDDs address space. The processor can relocate the register window in its address space at any time by changing the register window base address.

Fig. 4 : Memory Mapping



PRE-INITIALIZATION MEMORY MAPPING



POST-INITIALIZATION MEMORY MAPPING

REGISTER SEGMENT ORGANIZATION

PROCESSOR BYTE LOCATION (AFTER POWER UP)				VSDD BYTE LOC
0041EH	R15	HORIZ CONTROL REG 3	VERT CONTROL REG 3	1EH
"	R14	HORIZ CONTROL REG 2	VERT CONTROL REG 2	1CH
"	R13	HORIZ CONTROL REG 1	VERT CONTROL REG 1	1AH
"	R12	HORIZ CONTROL REG 0	VERT CONTROL REG 0	18H
"	R11	ACCESS TABLE BASE ADDRESS COUNTER		16H
"	R10	CHAR BASE ADDRESS 0 AND 1		14H
"	R9	COLOR TABLE BASE ADDRESS		12H
"	R8	ACCESS TABLE BASE ADDRESS		10H
"	R7	OBJECT DESCRIPTOR TABLE BASE ADDRESS		0EH
"	R6	PRIORITY ACCESS QUANTITY		0CH
"	R5	DATA SEGMENT BASE ADDRESS		0AH
"	R4	DATA WINDOW/SEGMENT BASE ADDRESS		08H
"	R3	DATA WINDOW BASE ADDRESS		06H
00404H	R2	REGISTER WINDOW BASE ADDRESS		04H
00402H	R1	VIDEO CONFIGURATION REGISTER 1		02H
00400H	R0	VIDEO CONFIGURATION REGISTER 0		00H

Video Configuration Register 0 (R0)		
Bit		Description
0	UCF	If set all registers will be updated after every frame. If not only ATBA and VCR0 will be updated.
1	DEI	Digital rather than analog output if set.
2	SAB	Slow (210 ns) rather than fast (140 ns) DRAM if set.
3	DEN	Enables VSDD display if set.
4	HRS	Resolution of up to 640 pixels per line, rather than 320 if set.
5	DOF	DRAM organisation, x4 if set, otherwise x1.
6-7	DAS1/2	DRAM array size, 256K, 64K or 16K bit chips.
8-12	BR4-0	Blink rate selection in multiples of 8 frame times.
13-15	DC2-0	Blink rate duty cycle time from 87.5 % to 12.5 %.

Video Configuration Register 1 (R1)		
Bit		Description
0	PRE	Pipeline read enable for MCS-51 family if set.
2	RE	Enables processor to read DRAM if set.
3	FAE	Reprograms RDY pin to Free Access indicator if set.
4	PCE	If set enables Priority Access counter, valid only with wait stable CPUs.
5	EVC	If set configures CKIO as input for pixel clock. If not outputs buffered clock.
6	VP	If set extends VSYNC pulse by half a line in interlace mode, for European TVs.
7	TMS	If set this VSDD is the slave in Twinmode.
8	TMM	If set this VSDD is the master in Twinmode.
9	SM	If set the VSDD outputs a composite sync signal, if not, sync is separate.
10	MAS	Master Sync, if set the VSDD generates the sync. If not the VSDD accepts sync from an external source.
11	INL	If set the VSDD generates an interlaced image.
12-15	CH3-0	Character height from 1 to 16 slices.

Register Segment (R2 - R15) Definition	
Register	Description
Register Window Base Address	This register (12 bits) contains the base address for the Register Window in the system processor address space. It may be placed on any 32 byte boundary.
Data Window Base Address	This register (5 bits) contains the base address for the Data Window in the system processor address space. It may be placed on a boundary corresponding to the size defined by the Data Window/Segment Length Mask register contents.
Data Window/ Segment Length Mask	This register (5 bits) contains the window segment length information, specifying 4K, 8K, 16K, 32K, 64K or 128K byte window size.
Data Segment Base Address	This register (7 bits) contains the base address of the VSDD memory space logically allocated to the system processor window. It may be placed on a boundary corresponding to the size defined by the Data Window/Segment Length Mask register contents.
Priority Access Quantity	This register contains the maximum number of system processor high priority accesses allowed during each scan line (4 bits).
Object Descriptor Table Base Address	This register (10 bits) contains the word base address of the Object Descriptor Table.
Access Table Base Address	This register (16 bits) contains the word base address of the Access Table. It is accessed by the VSDD every frame.
Color Table Base Address	This register (16 bits) contains the word base address of the color look-up table. It is accessed by the VSDD every frame.
Character Generator Base Addresses	These 2 registers (4 bits) contain the high order bits of the word base address of the character generators. Each base address represents a contiguous character generator.
Access Table Base Address Counter	This register is maintained by the VSDD as a pointer to the next Access Table entry. The system processor can read this value to determine the next line to be processed, but should never write to it.
Screen Timing Constants	The four registers from 18H to 1EH hold data for the screen timing constants. Four constants are defined for vertical and horizontal timing.

ACCESS TABLE

The Access Table contains the vertical window information for each object. It is organised as 512 registers of 16 bits, each bit representing an object and each register representing a scan line. An object is activated by putting a zero in the scan line corresponding to the start and stop lines of the object. The Access Table begins at the address defined in the Access Table Base Address (ATBA) register. Different Access Tables may be defined at the same time but only one is activated during a frame. The Access Table allows easy vertical scrolling of an object. If the object is scrolled downwards truncating will take place automatically when the object goes out of the screen. Scrolling upwards is similar except that when the object goes out of the top of the screen, the object base address must be incremented to point to the start of the next line.

OBJECT DESCRIPTOR TABLE

The Object Descriptor Table (ODT) is a 4 word field per object that describes the basic object characteristics, such as the base address, attributes and X position. This information is initialised and updated by the system processor. The 16 available object descriptors (64 words) are located contiguously in the Object Descriptor Table at the location specified in the Object Descriptor Table Base Address (ODTBA) register.

Each object is described as either a bit-map or character object. Based on this information each object is decoded accordingly by the VSDD. A bit in one of the four words determines whether an object is bit-map or character. Table 4 describes the data stored for each type of object within the ODT.

Table 4 : Object Descriptor Contents.

Character Objects	Bit Map Objects
Character width fixed at 6, 8, 12 or 16 pixels/character or proportional spacing.	Object resolution 8, 4 or 2 bits/pixel.
Defines if 1 or 3 bytes are used per character.	Object bank selection.
Character color resolution, 8 or 16 colors can be specified.	Object blink bit.
Character generator to be selected.	Transparent pixel detection.
X0 coordinated of object.	Default color specification.
	X0 coordinate of object.
	Object base address and current object entry address

OBJECT DATA

Data for all objects, bit-map and character, are stored in VSDD DRAM starting at the address defined in the Object Descriptor Table. This table contains an entry for each of the 16 possible objects that the VSDD can process at any one time.

The length of the object data is determined by the object width and resolution. As the width of an object is a multiple of four 16 bit words, some limitations exist concerning object widths.

Object Type	Min. Width	Max. Width
Bit map 2 bits/pixel	32 pixels	2048 pixels
Bit map 4 bits/pixel	16 pixels	1024 pixels
Bit map 8 bits/pixel	3 pixels	512 pixels
Character 1 byte/character	3 chars	512 chars
Character 3 byte/character	1 char **	170 chars *

* The last 16 bit word of the object will not be used.
** The minimum memory required is 4 words. The second character would have transparent attributes. As above the last 16-bit word would not be used.

For character objects two formats are defined. The first is a 1 byte/character mode, in this mode two ASCII characters are stored in each DRAM word.

1 BYTE / CHARACTER

X15	X0
2nd character	1st character
A7:A6:A5:A4:A3:A2:A1:A0	A7:A6:A5:A4:A3:A2:A1:A0

The second format uses 3 bytes/character. They are formed as follows :

3 BYTES / CHARACTER

X15		X0	
2nd character attribute field			high address
1st character attribute field			
A7:A6:A5:A4:A3:A2:A1:A0		A7:A6:A5:A4:A3:A2:A1:A0	low address
2nd character		1st character	

The attribute field is formatted as follows :

CG:TFG:TBG:DW:MSK:INV:BLI:UND:FC3:FC2:FC1:FC0:BC3:BC2:BC1:BC0

Where :

A7-A0	8 bit ASCII code
BC2-BC0	Background color
BC3 [U/L]	Is used to specify the upper or lower half of the character in double height mode, or is used as the MSB of the background color.
FC2-FC0	Foreground color.
FC3 [DH]	Is used to specify whether the character is double height, or is used as the MSB of the foreground color.
UND	Underlines the character if set.
BLI	Blinks the character if set.
INV	Inverts the foreground and background colors of the character if set.
MSK	Masks the character if set (Conceal/Reveal).
DW	Doubles the width of the character if set.
TBG	Background color is transparent if set.
TFG	Foreground color is transparent if set.
CG	Selects one of the two character generators.

CHARACTER GENERATORS

The VSDD can support two sets of character generators with 256 characters per set. Since characters are defined in DRAM, a new version of the character generator can be updated by either :

- modifying the character generator directly ;
- updating one set while the other set is being displayed. The set can then be changed by updating the Character Generator Base Address pointer in the register segment. This results in an instantaneous change to the screen.

Each character set requires 256 x H words of DRAM, where H is the height of the characters. Each character consists of H slices with slice zero defined as the bottom of the character. The slice information is always stored with the leftmost pixel in the low bits of the memory location. A bit set to one (1) designates a pixel with foreground color, as defined by the attribute field in 3 byte/char mode, or by the Object Descriptor Table in 1 byte/char mode.

PICTURE CONSTRUCTION

The VSDD can support picture sizes of up to 320 x 512 or 640 x 512 pixels using 8, 4 or 2 bit pixels in the first mode and 2 or 4 bit pixels in the second. In the 8 bit pixel mode only the bottom four bits are used by the internal color look-up table. This mode is useful in digital operation when more than 16 colors are required. The VSDD can the be connected directly to an external color palette.

The VSDD starts picture construction at the beginning of the frame, and does the following for each line using the logic flow show in figure 5.

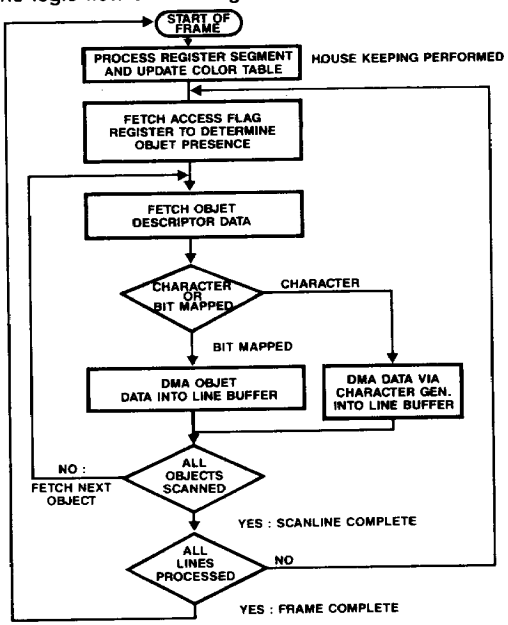


Figure 6 shows how objects are accessed indirectly by means of tables. The main table is the Object Descriptor Table (ODT) that contains information for all the on-screen objects. The address of this table is given in the register segment. Each entry contains information concerning the type of object, its size, attributes and X coordinate. Character objects are specified with other information such as the character generator to be used.

In conjunction with this table there is also the Access Flag Table (AFT). The AFT contains an entry of 16 bits for each of the scan lines. Each object is assigned to a bit within the word. A bit set at a zero will toggle the display of a particular object, enabling objects to be turned on and off as required. The first bit at zero will turn the object on and display will start from the beginning of the object. The second bit will turn the object off. This bit is normally at the end of an object, but may be earlier to truncate objects.

Movement of objects is accomplished easily in the X direction by changing the value in the object descriptor. Movement in the Y direction causes no problems until the object starts to move off screen. If the object is moving down the bit that turns on the object will gradually descend in the AFT as the object moves off-screen, the object being automatically truncated. Moving off-screen in an upward direction is the same except that when the object moves off-screen the object base address in the descriptor table must be changed to truncate the top of the object.

The VSDD uses two pixel line buffers to overlap line construction and display. The free pixel buffer is filled with object information while the other buffer is being displayed. For bit-map objects the information passes directly into the buffer. Character objects pass via a character generator first. Up to two character generators of 256 characters may be defined in RAM. Characters may be as small as 2 x 2 pixels up to a maximum of 16 x 16 pixels. The height of characters is defined globally for the display but the width may be variable depending upon the mode selected. The size of variable width character is from 2 to 14 pixels, this allows proportional spacing as seen on word processing units.

There are two types of character object, 1 byte/character and 3 bytes/character. The first allows display of characters in the color and with the attributes specified in the descriptor. The second allows attributes to be defined for each individual character, allowing greater flexibility but using more memory and greater bandwidth.

Bit map objects have their attributes set in the descriptor, but the pixel color is determined by its value. Four bit pixels allow 16 colors and two bit pixels allow four colors. All colors of all objects are also subject to translation. The VSDD contains a color table consisting of 16 entries, these are the logical colors. Each logical color is related to an actual color which is defined in 12 bits, 4 bits for each of the primary colors. The color table is reloaded at the end of each frame so that extra blinking modes or color changes between frames can be added if necessary. One of possible colors available is "transparent", this allows objects with lower priorities to be seen through an object that covers it. This

facility coupled with the ability to define the foreground and background colors allows portions of objects to be hidden on the screen. The color Look-up Table is defined by the user and stored in RAM. Again the register segment contains a pointer to its address allowing the table to be changed easily.

As the process of writing to the pixel line buffer is done one object after another, the last object will overwrite prior objects, except where transparent pixels are defined. This gives an object an ascending priority with object number. For example object 5 has a higher priority than object 3. Each line is constructed in a similar manner up to 512 times par frame.

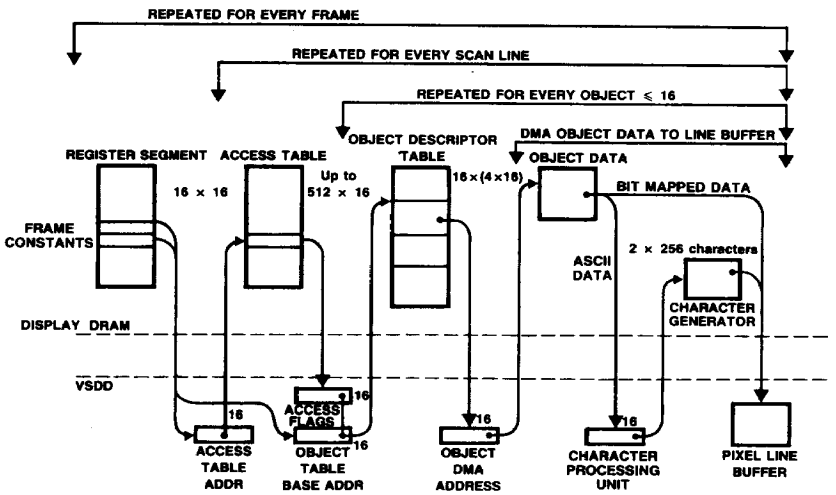


Fig. 6 : VSDD Memory Organisation.

SYNCHRONIZATION AND SYSTEM TIMING

Several registers in the register segment contain various constants that are used to hold timing information for the display. This method allows the VSDD to be compatible with virtually any monitor or television standard. The synchronization output of the VSDD appears on the vertical and horizontal output pins. Alternatively, the VSDD is capable of generating a composite synchronization output. Both types of synchronization are available with interlaced or non-interlaced field information. The VSDD will output the same image for both fields in interlace mode.

When the VSDD is used to overlay digital images on a TV or VCR picture the two sources must be locked together. The VSDD is capable of accepting external synchronization on the horizontal and vertical pins, which are reconfigured as inputs. As above both composite and interlaced signals can be used. The VSDD contains its own phase comparator which can be used to complete a full Phase-Locked Loop to ensure picture stability. The Incrustation output, in conjunction with the color look-up table, is used to carry out picture source switching.

TWIN-MODE OPERATION

For higher performance it is possible to connect two VSDD chips in parallel. One of them is designated as the master and the other as the slave. The master generates information for the even lines of the display together with all the system timing. The slave accepts the synchronization pulses as inputs and displays the odd lines of the picture. Because each VSDD is essentially constructing half the picture the time allowed is twice as great, allowing higher throughput in terms of information processed and objects displayed.

SEMI-GRAPHIC AND VIDEOTEX APPLICATIONS

Although the VSDD supports full bit map graphics, the character modes, notably 3 bytes/character allow the VSDD to support semi-graphic and Videotex applications with a minimum software overhead. As character are held in RAM, users are free to design the characters they wish, so the VSDD can be used for any semi-graphics application using characters of up to 16 x 16 pixels.

The VSDD can support several different Videotex standards including European, North American and Japanese standards. Although it has been optimised for alpha-geometric applications that use bit maps (NAPLPS, GKS, VDI) it is capable of supporting the existing alpha-mosaic standards.

It can directly support most of the European CEPT standard (levels 1, 2 and 3), that includes PRESTEL and TELETEL, using character objects, in addition to having bit-map objects and movement. Alpha-photographic standards such as Picture PRESTEL and Picture TELETEL can be supported in 8 bit pixel mode with the addition of external color translation and higher resolution hardware.

PERFORMANCE

The number of objects that the VSDD can support on a scan line is dependent upon the screen resolution, refresh rate, DRAM access time and object resolution. In addition the percentage overlap of each object can affect the performance.

Figure 7 illustrates the maximum number of pixels that a VSDD can treat on a single scan line for various numbers of objects. All objects are bit mapped at 4 bits/pixel and the frame rate is 50 Hz non-interlaced. As shown at the maximum resolution of 512 lines, a single VSDD displaying 2 objects can treat around 800 pixels per line. This allows a full-screen object of 640 pixels plus slightly smaller object(s) to be displayed. All objects will be displayed correctly as long as the total number of pixels in all objetcs does not exceed 800 in a single scan line. At a resolution of 256 lines with 4 objects, around 1700 pixels may be treated. At a horizontal resolution of 320 pixels this allows four full-screen objects per scan line. Each object requires 320 pixels, making 1280 in all for four objects.

In both cases the capability of the VSDD is not exceeded and so the objects may be placed anywhere on the screen with any amount of overlap, without encountering any display problems. Note that the number of lines per frame includes the vertical blanking time. Note also that these values are doubled if 2 bit pixels are used.

If the number of pixels to be handled exceeds the capacity of the VSDD, say trying to handle four objects of 640 pixels with a resolution of 640 × 256, the VSDD will activate the CTO signal. The CTO, Construction Time Overflow, can be used to interrupt the processor to inform it that the image has not been correctly formed. The system software can then deal with the problem.

If 2 bit/pixel objects are used, the values on the Y-axis, number of pixels treated, are effectively doubled. So at 320 by 256 up to 8 2 bit/pixel objects could be supported on the same line.

A significant performance increase can be seen when two VSDDs are used in twin mode. At full resolution and with slow RAMs, 7 objects can be supported per scan line. The effect of going to twin mode allows each VSDD twice as long to construct the line.

At the start of each line the VSDD performs housekeeping functions such as updating internal registers from the register segment in DRAM. This requires 6.3 uS of the scan line time, with a 14.5 MHz system clock. In addition, each object displayed on the scan line requires 3.5 uS to fetch and decode the attributes in the Object Descriptor Table. The time left is used to DMA the object data into the pixel line buffer. Each bit map data word transferred can contain 2, 4 or 8 pixels depending upon the object resolution.

Character objects require the same amount of object overhead, but the time to fetch a character slice (see Character Generator section) is dependent upon the number of bytes per character and the memory access time. The character slice access time is defined below.

Bytes/Character	Memory Type	Access Time
1	slow	0.56 uS
1	fast	0.49 uS
3	slow	0.74 uS
3	fast	0.56 uS

The VSDD combined with a CPU and DRAM offers a simple yet powerful solution to a variety of applications. By choosing the CPU, DRAM and VSDD mode of operation, a wide range of screen resolutions and object windows can be supported.

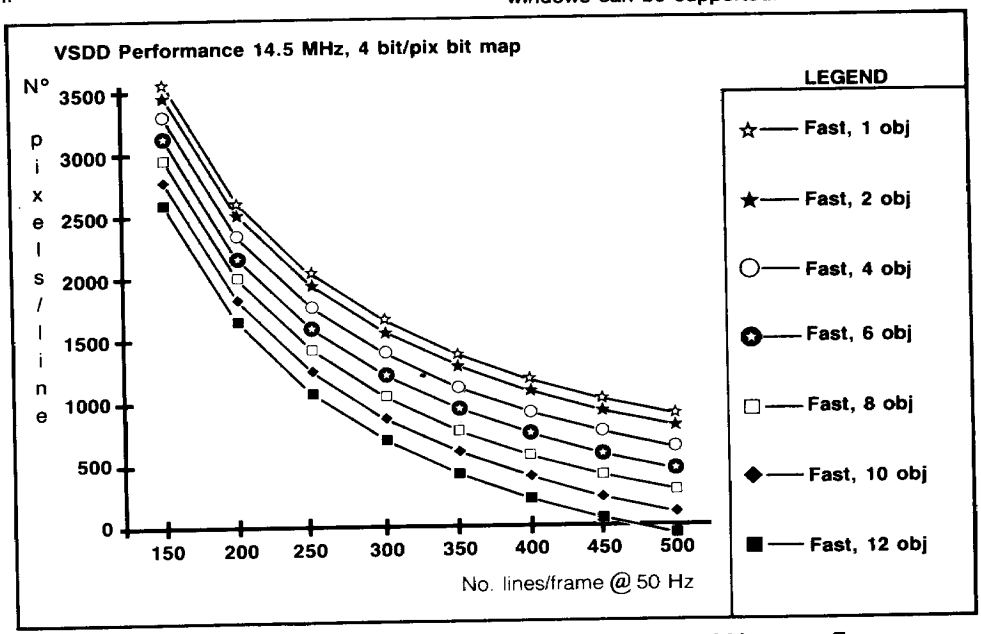
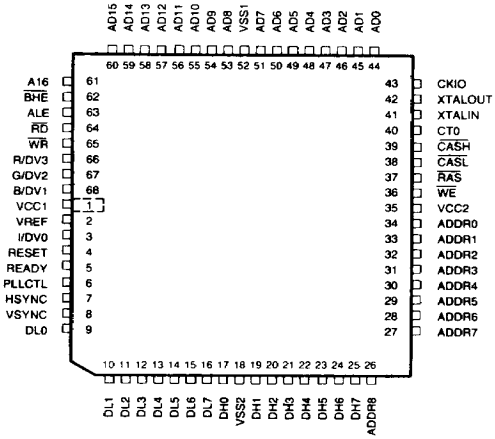


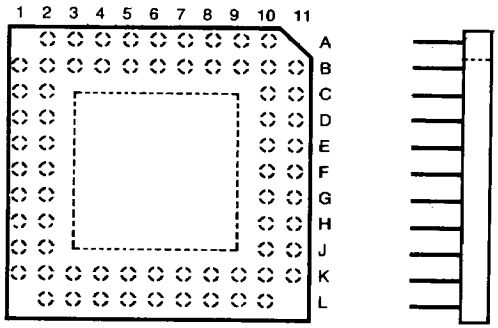
Fig. 7 : Number of Pixels Handled per Line Versus Number of Lines per Frame.

Packaging (TOP VIEWS)

The VSDD is available in a 68 lead plastic leaded chip carrier and in a 68-pin pin grid array.



PLCC/LCC DIE DOWN



PGA DIE DOWN (68 PIN)

DES.	PLCC PIN N°	PGA PIN N°	DES.	PLCC PIN N°	PGA PIN N°	DES.	PLCC PIN N°	PGA PIN N°	DES.	PLCC PIN N°	PGA PIN N°
VCC1	1	F11	VSS2	18	A6	VCC2	35	F1	VSS1	52	L6
VREF	2	F10	DH1	19	B6	$\overline{WE}$	36	F2	AD8	53	K6
I/DV0	3	E11	DH2	20	A5	$\overline{RAS}$	37	G1	AD9	54	L7
RESET	4	E10	DH3	21	B5	$\overline{CASL}$	38	G2	AD10	55	K7
READY	5	D11	DH4	22	A4	$\overline{CASH}$	39	H1	AD11	56	L8
PLLCTL	6	D10	DH5	23	B4	CT0	40	H2	AD12	57	K8
HSYNC	7	C11	DH6	24	A3	XTALIN	41	J1	AD13	58	L9
VSYNC	8	C10	DH7	25	B3	XTALOUT	42	J2	AD14	59	K9
DL0	9	B11	ADDR8	26	A2	CKI0	43	K1	AD15	60	L10
DL1	10	A10	ADDR7	27	B1	AD0	44	L2	A16	61	K11
DL2	11	B10	ADDR6	28	B2	AD1	45	K2	$\overline{BHE}$	62	K10
DL3	12	A9	ADDR5	29	C1	AD2	46	L3	ALE	63	J11
DL4	13	B9	ADDR4	30	C2	AD3	47	K3	$\overline{RD}$	64	J10
DL5	14	A8	ADDR3	31	D1	AD4	48	L4	$\overline{WR}$	65	H11
DL6	15	B8	ADDR2	32	D2	AD5	49	K4	R/DV3	66	H10
DL7	16	A7	ADDR1	33	E1	AD6	50	L5	G/DV2	67	G11
DH0	17	B7	ADDR0	34	E2	AD7	51	K5	B/DV1	68	G10

5

Ordering Information